TOSHIBA RISC PROCESSOR

TMPR3922AU

(32-bit RISC Microprocessor)

1. GENERAL DESCRIPTION

The TMPR3922AU is a single-chip integrated digital ASSP for PDA(Personal Digital Assistants). The TMPR3922AU consists of PDA system support logic, integrated with the TX3920 processor Core designed by Toshiba.

2. FEATURES

- R3000A-based TX3920 Processor Core
  - RISC architecture developed by The MIPS Group, a division of Silicon Graphics, Inc.
  - Toshiba has added its own multiply-add and branch-likely instructions.
  - A single-cycle multiply/accumulate module to allow integrated DSP functions, such as a software modem for high-performance standard data and fax protocols
  - Instruction cache: 16K bytes(2Way); data cache : 8K bytes(2Way)
  - On-chip Translation Lookaside Buffer (TLB) with 64×64-bit wide entries, each of which maps 4K/16K/64K/256K/1M/4M Byte page
  - Max 129MHz operation
- Built-in peripheral circuit
  - Clock generator with built-in sixteenfold-frequency phase-locked loop (PLL)
  - Four-stage write buffer
  - A high performance and flexible Bus Interface Unit
  - Multiple DMA channels
  - Memory controller for DRAM(EDO), SDRAM, SRAM, ROM, Flash Memory and PCMCIA
  - Power management unit
  - Big / Little endian
- Low power dissipation
  - 3.3V(I/O) / 2.7V(Internal) operation
  - Standby Current 50μA(typ)
  - CPU clock stop mode
  - Power down modes for individual internal peripheral modules
- Plastic LQFP 208-pin package

3. SYSTEM CONFIGURATION

3.1 SYSTEM BLOCK DIAGRAM

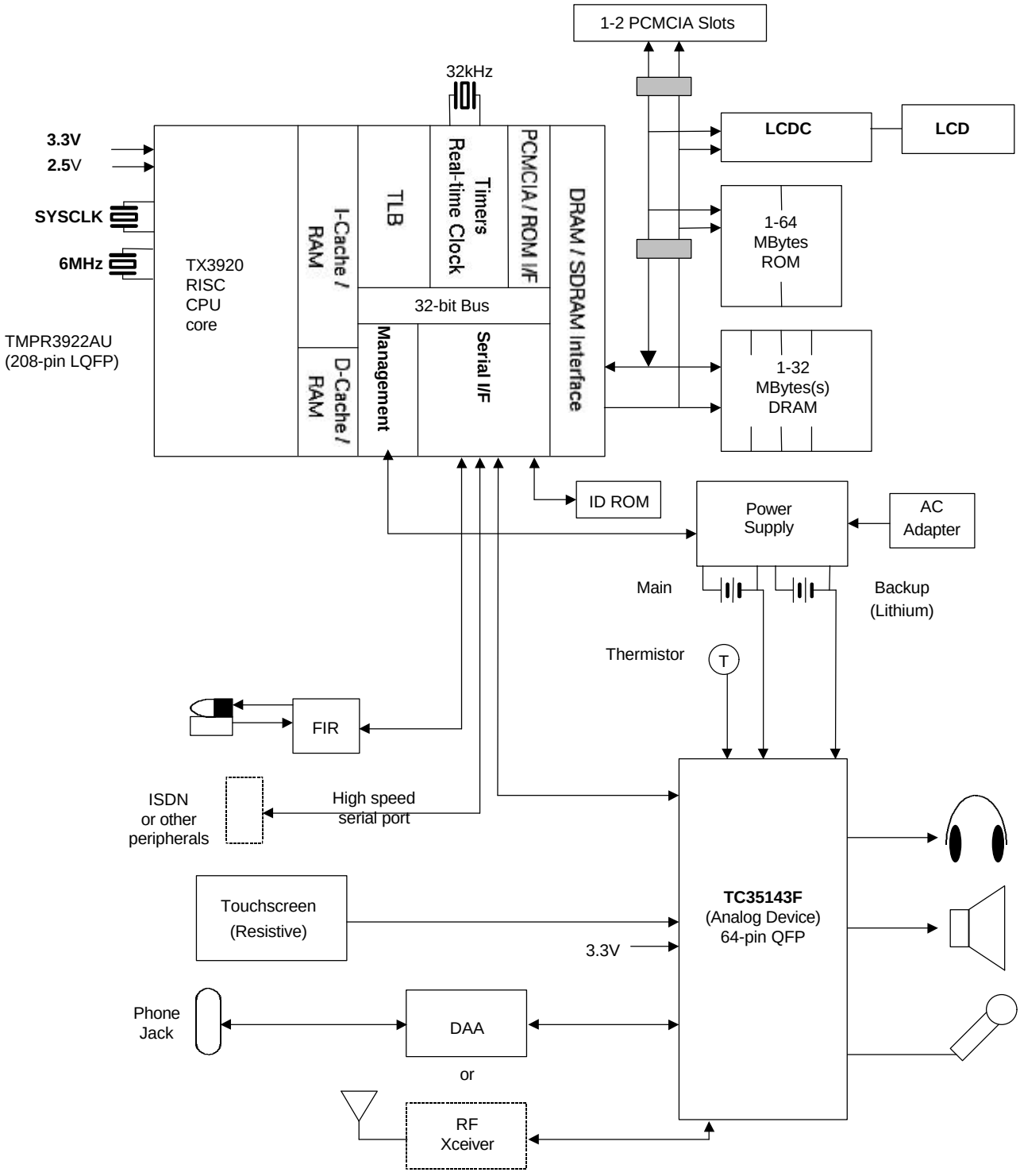


FIG. 3.1 SYSTEM BLOCK DIAGRAM

3.2 TMPR3922AU DIAGRAM

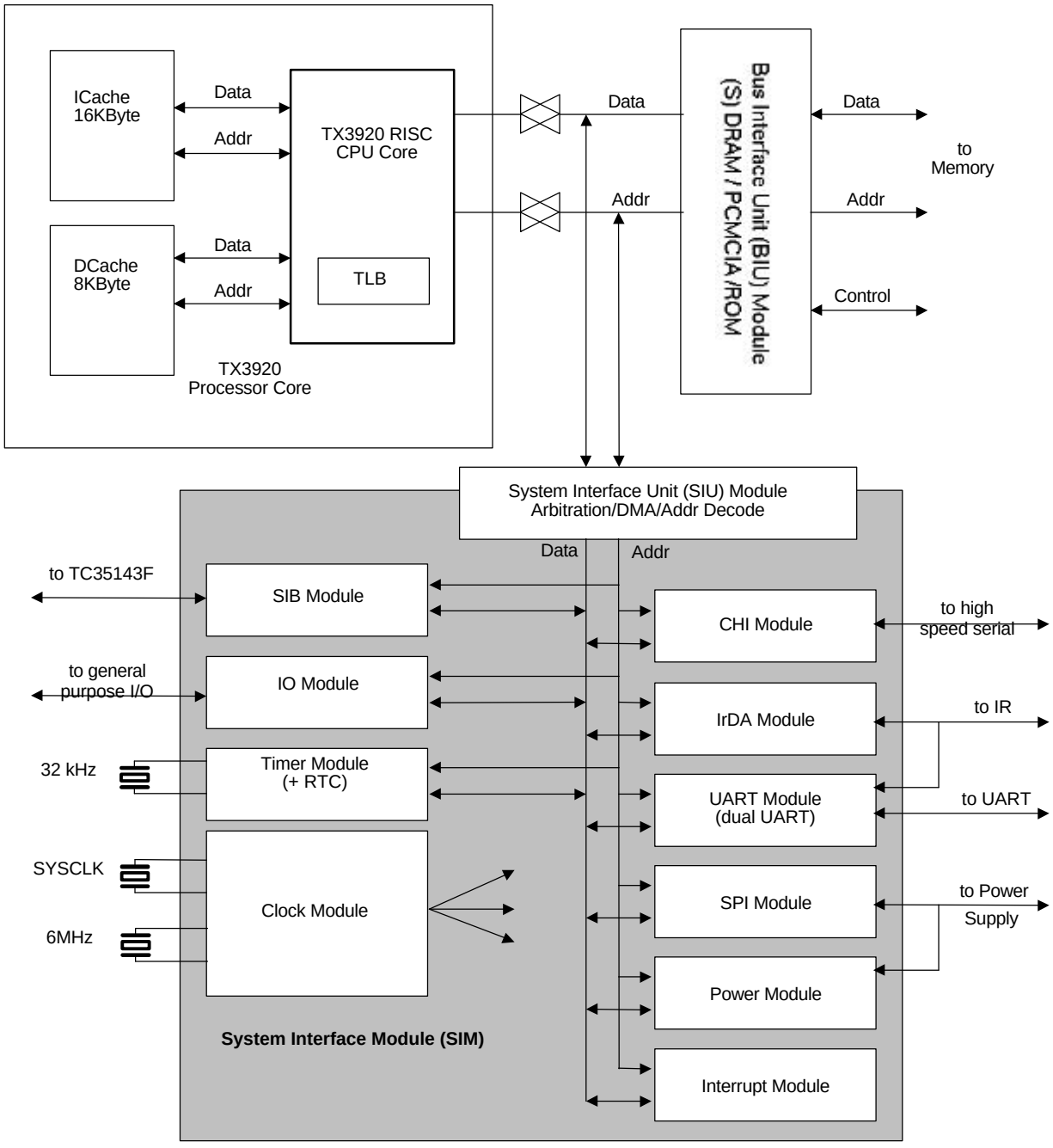


FIG. 3.2 TMPR3922AU BLOCK DIAGRAM

3.3 MEMORY CONNECTIONS

D [31:0] Data Bus and CAS* signals change the name of the pins in the Little Endian mode as follows.

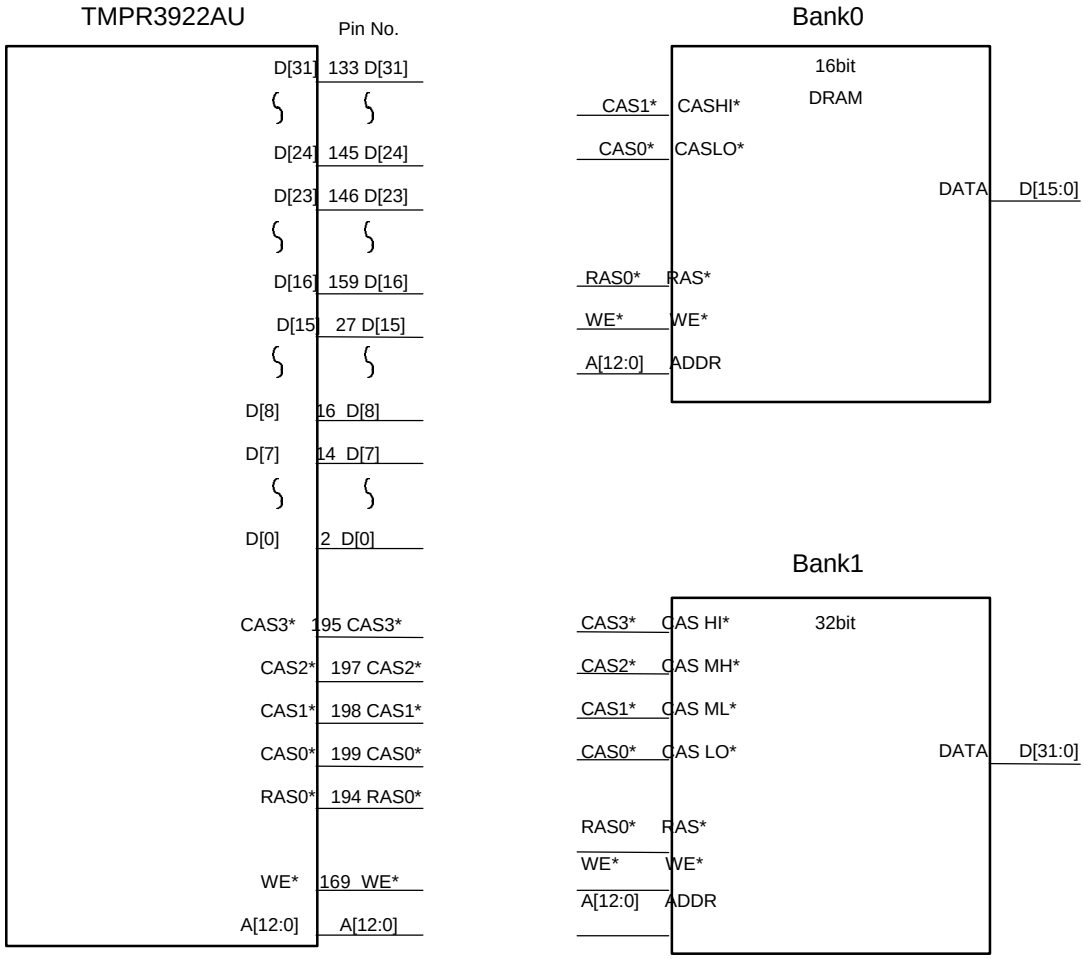
D [31:24]	becomes	D[7:0]
D [23:16]	becomes	D[15:8]
D [15:8]	becomes	D[23:16]
D [7:0]	becomes	D[31:24]

CAS3*	becomes	CAS0*
CAS2*	becomes	CAS1*
CAS1*	becomes	CAS2*
CAS0*	becomes	CAS3*

<Note>

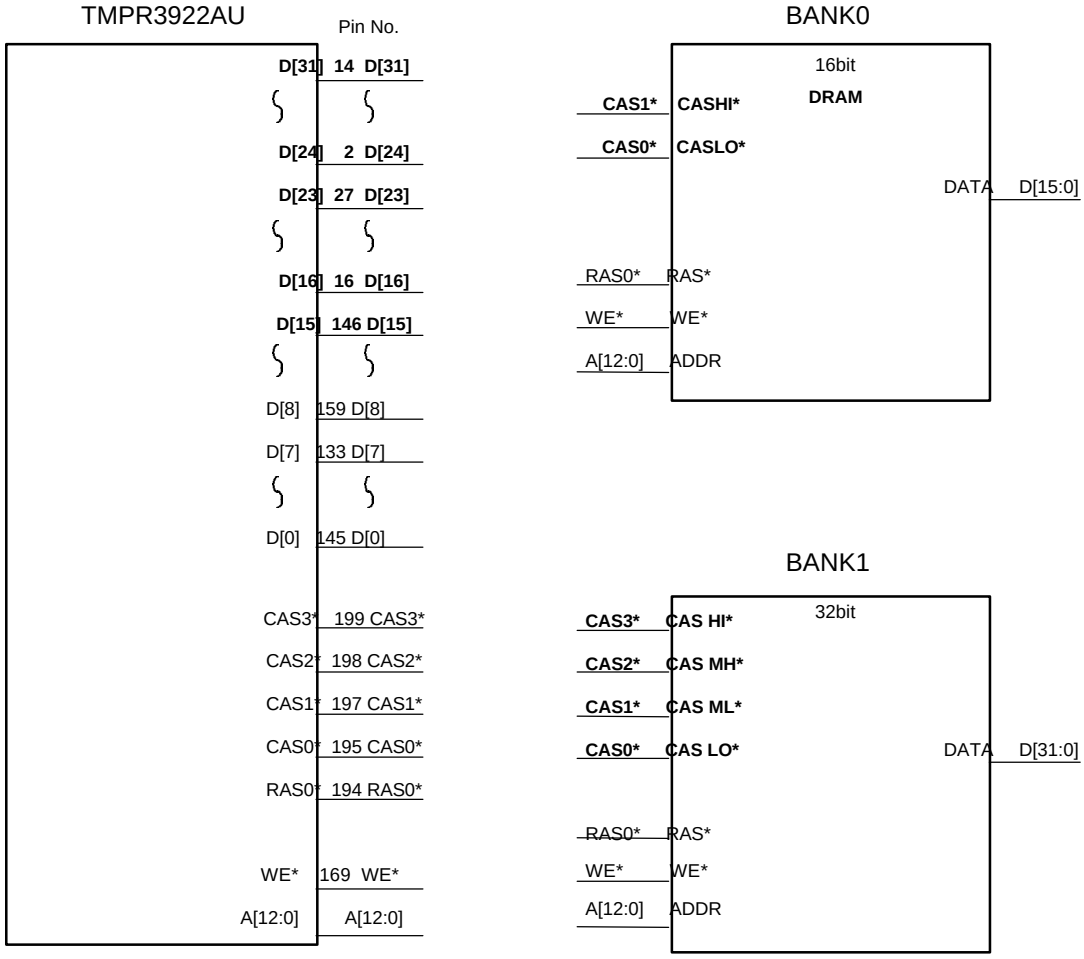
The connection between the TMPR3922AU and Memory depends on the endianess.

3.3.1 MEMORY CONNECTIONS (Big Endian)



Big Endian

3.3.2 MEMORY CONNECTIONS (Little Endian)



Little Endian

4. PINS

4.1 PIN ASSIGNMENT

NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME
1	–	VDDH	41	I	SIBDIN	81	–	VSS
2	I/O	D[0] (D [24])	42	O	SIBDOUT	82	O	PWRCS
3	–	VSS	43	–	VDDH	83	I	PWRINT
4	I/O	D[1] (D [25])	44	I	SIBIRQ	84	I	PWROK
5	I/O	D[2] (D [26])	45	I/O	I/O[13]	85	I/O	IO[8]
6	–	VDDL	46	I/O	I/O[14]	86	I	ONBUTN
7	I/O	D[3] (D [27])	47	I/O	I/O[15]	87	I	PON*
8	–	VSS	48	–	VSS	88	I	CPURES*
9	I/O	D[4] (D [28])	49	I/O	CHICLK	89	–	VDDL
10	–	VDDLS	50	I/O	CHIFS	90	I	C6MIN
11	I/O	D[5] (D [29])	51	I	CHIDIN	91	O	C6MOUT
12	I/O	D[6] (D [30])	52	O	CHIDOUT	92	–	VSS
13	–	VSS	53	–	VDDH	93	I/O	IO[9]
14	I/O	D[7] (D [31])	54	I	RXD	94	I/O	IO[10]
15	–	VSS	55	O	TXD	95	I/O	IO[11]
16	I/O	D[8] (D [16])	56	I	IRINA	96	–	VSSP(PLL)
17	–	VDDH	57	I	IRINB	97	–	VDDP(PLL)
18	I/O	D[9] (D [17])	58	O	FIROUT	98	O	C48MOUT
19	I/O	D[10] (D [18])	59	O	IROUT	99	I/O	IO[7]
20	–	VSS	60	–	VSS	100	I/O	IO[6]
21	I/O	D[11] (D [19])	61	–	VDDH	101	I/O	IO[5]
22	–	VDDH	62	I	CARDET	102	–	VSSP(PLL)
23	I/O	D[12] (D [20])	63	O	RXPWR	103	I/O	IO[1]
24	I/O	D[13] (D [21])	64	I/O	IO[3]	104	–	VDDP(PLL)
25	–	VSS	65	I/O	IO[2]	105	I	CARD2WAIT*
26	I/O	D[14] (D [22])	66	–	VSS	106	O	CARD2CSH*
27	I/O	D[15] (D [23])	67	O	SPICLK	107	O	CARD2CSL*
28	–	VDDL	68	I	SPIIN	108	I/O	IO[0]
29	I	ENDIAN	69	O	SPIOUT	109	–	VSS
30	NC	RESERVED	70	–	VDDLS	110	O	CARDIORD*
31	NC	RESERVED	71	I	TESTCPU	111	O	CARDIOWR*
32	NC	RESERVED	72	I	TESTIN	112	O	CARDREG*
33	–	VSS	73	O	BCLK	113	I	CARD1WAIT*
34	NC	RESERVED	74	I	TESTAIU	114	–	VDDH
35	I/O	IO[12]	75	–	VSS	115	O	CARDDIR*
36	–	VDDLS	76	I	VCC3	116	–	VDDLS
37	O	SIBMCLK	77	O	BC32K	117	O	CARD1CSL*
38	–	VSS	78	–	VDDL	118	O	CARD1CSH*
39	O	SIBSCLK	79	I	C32KIN	119	–	VSS
40	O	SIBSYNC	80	O	C32KOUT	120	I	MCS1WAIT*

*Active-low signal ( ) indicates the signal name in the Little endian mode

NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME
121	I	MCS0WAIT*	161	I/O	IO[4]	201	–	VDDL
122	O	MCS1*	162	O	CS0*	202	O	DCKE
123	O	MCS0*	163	O	RD*	203	–	VSS
124	O	CS3*	164	–	VSS	204	I	DCLKIN
125	O	CS2*	165	–	VDDLS	205	O	DCLKOUT
126	O	CS1*	166	O	DGRNT*	206	–	VDDH
127	–	VDDL	167	I	DREQ*	207	O	DQMH
128	I	SYSCLKIN	168	O	ALE	208	O	DQML
129	O	SYSCLKOUT	169	O	WE*			
130	–	VSS	170	–	VDDH			
131	–	VSS	171	I/O	A[12]			
132	–	VDDLS	172	I/O	A[11]			
133	I/O	D[31] (D [7])	173	–	VSS			
134	I/O	D[30] (D [6])	174	I/O	A[10]			
135	–	VSS	175	I/O	A[9]			
136	I/O	D[29] (D [5])	176	–	VDDL			
137	–	VDDH	177	I/O	A[8]			
138	I/O	D[28] (D [4])	178	I/O	A[7]			
139	I/O	D[27] (D [3])	179	–	VSS			
140	–	VSS	180	I/O	A[6]			
141	I/O	D[26] (D [2])	181	I/O	A[5]			
142	–	VSS	182	–	VDDH			
143	I/O	D[25] (D [1])	183	I/O	A[4]			
144	–	VDDLS	184	–	VSS			
145	I/O	D[24] (D [0])	185	I/O	A[3]			
146	I/O	D[23] (D [15])	186	I/O	A[2]			
147	–	VDDH	187	–	VDDL			
148	I/O	D[22] (D [14])	188	I/O	A[1]			
149	–	VSS	189	I/O	A[0]			
150	I/O	D[21] (D [13])	190	–	VSS			
151	–	VDDH	191	–	VSS			
152	I/O	D[20] (D [12])	192	O	DCS0*			
153	I/O	D[19] (D [11])	193	O	RAS1*			
154	–	VSS	194	O	RAS0*			
155	I/O	D[18] (D [10])	195	O	CAS3* (CAS0*)			
156	–	VDDLS	196	–	VDDH			
157	I/O	D[17] (D [9])	197	O	CAS2* (CAS1*)			
158	–	VSS	198	O	CAS1* (CAS2*)			
159	I/O	D[16] (D [8])	199	O	CAS0* (CAS3*)			
160	–	VDDH	200	–	VSS			

*Active-low signal ( ) indicates the signal name in the Little endian mode

4.2 PIN FUNCTIONS

- Memory Pins

NAME	I/O	DESCRIPTION
D[31:0]	I/O	These pins are the data bus for the system. 16-bit SDRAMs and DRAMs should be connected to bits 15:0. All other 16-bit ports should be connected to bits 31:16. Of course, 32-bit ports should be connected to be bits 31:0. These pins are normally outputs and only become inputs during reads, thus no resistors are required since the bus will only float for a short period of time during bus turn-around.
A[12:0]	O	These pins are the address bus for the system. The address lines are multiplexed and can be connected directly to SDRAM and DRAM devices. To generate the full 26-bit address for static devices, an external latch must be used to latch the signals using the ALE signal. For static devices, address bits 25:13 are provided by the external latch and address bits 12:0 (directly connected from the TMPR3922AU's address bus) are held afterward by the TMPR3922AU for the remainder of the address bus cycle.
ALE	O	This pin is used as the address latch enable to latch A[12:0] using an external latch, for generating the upper address bits 25:13.
RD*	O	This pin is used as the read signal for static devices. This signal is asserted for reads from MC3*-0*, CS3*-0*, CARD2CS* and CARD1CS* for memory and attribute space, and for reads from the TMPR3922AU accesses if SHOWDINO is enabled (for debugging purposes) .
WE*	O	This pin is used as the write signal for system. This signal is asserted for writes to MC3*-0*, CS3*-0*, CARD2CS* and CARD1CS* for memory and attribute space, and for writes to DRAM and SDRAM.
CAS0*(WE0*)	O	This pin is used as the CAS signal for SDRAMs, the CAS signal for D[7:0] for DRAMs, and the write enable signal for D[7:0] for static devices.
CAS1*(WE1*)	O	This pin is used as the CAS signal for D[15:8] for DRAMs, and the write enable signal for D[15:8] for static devices.
CAS2*(WE2*)	O	This pin is used as the CAS signal for D[23:16] for DRAMs, and the write enable signal for D[23:16] for static devices.
CAS3*(WE3*)	O	This pin is used as the CAS signal for D[31:24] for DRAMs, and the write enable signal for D[31:24] for static devices.
RAS0*	O	This pin is used as the RAS signal for SDRAMs and the RAS signal for Bank0 DRAMs.
RAS1*(DCS1*)	O	This pin is used as the chip select signal for Bank1 SDRAMs and the RAS signal for Bank1 DRAMs.

*Active-low signal

NAME	I/O	DESCRIPTION
DCS0*	O	This pin is used as the chip select signal for Bank0 SDRAMs.
DCKE	O	This pin is used as the clock enable for SDRAMs.
DCLKIN	I	This pin must be tied externally to the DCLKOUT signal and is used to match skew for the data input when reading from SDRAM and DRAM devices.
DCLKOUT	O	This pin is the (nominal) 73.728MHz clock for the SDRAMs.
DQMH	O	This pin is the upper data mask for a 16-bit SDRAM configuration.
DQML	O	This pin is the lower data mask for a 16-bit SDRAM or an 8-bit SDRAM configuration.
CS3-0*	O	These pins are the Chip Select 3 through 0 signals. They can be configured to support either 32-bit or 16-bit ports.
MCS1-0*	O	These pins are the Chip Select 1 through 0 signals for the external device. They can be configured to support either 32-bit or 16-bit ports.
CARD2CSH*, L*	O	These pins are the Chip Select signals for PCMCIA card slot 2.
CARD1CSH*, L*	O	These pins are the Chip Select signals for PCMCIA card slot 1.
CARDREG*	O	This pin is the REG* signal for the PCMCIA cards.
CARDIORD*	O	This pin is the IORD* signal for the PCMCIA IO cards.
CARDIOWR*	O	This pin is the IOWR* signal for the PCMCIA IO cards.
CARDDIR*	O	This pin is used to provide the direction control for bi-directional data buffers used for the PCMCIA slot(s). This signal will assert whenever CARD2CSH* or CARD2CSL* or CARD1CSH* or CARD1CSL* is asserted and a read transaction is taking place.
CARD2WAIT*	I	This pin is the card wait signal from PCMCIA card slot 2.
CARD1WAIT*	I	This pin is the card wait signal from PCMCIA card slot 1.
MCS1WAIT*	I	This pin is the wait signal from the external device 1.
MCS0WAIT*	I	This pin is the wait signal from the external device 0.

*Active-low signal

- Bus Arbitration Pins

NAME	I/O	DESCRIPTION
DREQ*	I	This pin is used to request external arbitration. If the TESTAIU signal is high and the TESTAIU function has been enabled, then once DGRNT* is asserted, external logic can initiate reads or writes to the TMPR3922AU registers by driving the appropriate input signals. If the TESTAIU signal is low or the TESTAIU function has not been enabled, then the TMPR3922AU memory transactions are halted and certain memory signals will be tri-stated when DGRNT* is asserted in order to allow an external master to access memory.
DGRNT*	O	This pin is asserted in response to DREQ* to inform the external test logic or bus master that it can now begin to drive signals.

*Active-low signal

- Clock Pins

NAME	I/O	DESCRIPTION
SYSCLKIN	I	This pin should be connected along with SYSCLKOUT to an external crystal which is the main TMPR3922AU clock source.
SYSCLKOUT	O	This pin should be connected along with SYSCLKIN to an external crystal which is the main TMPR3922AU clock source.
C32KIN	I	This pin along with C32KOUT should be connected to a 32.768 kHz crystal.
C32KOUT	O	This pin along with C32KIN should be connected to a 32.768 kHz crystal.
C6MIN	I	This pin along with C6MOUT should be connected to a 6 MHz crystal.
C6MOUT	O	This pin along with C6MIN should be connected to a 6 MHz crystal.
C48MOUT	O	This pin is a buffered output of the 48 MHz clock.
BC32K	O	This pin is a buffered output of the 32.768 kHz clock.
BCLK	O	This pin is a reference clock for the external device.

- CHI Pins

NAME	I/O	DESCRIPTION
CHIFS	I/O	This pin is the CHI frame synchronization signal. This pin is available for use in one of two modes. As an output, this pin allows the TMPR3922AU to be the master CHI sync source. As an input, this pin allows an external peripheral to be the master CHI sync source and the TMPR3922AU CHI module will slave to this external sync.
CHICLK	I/O	This pin is the CHI clock signal. This pin is available for use in one of two modes. As an output, this pin allows the TMPR3922AU to be the master CHI clock source. As an input, this pin allows an external peripheral to be the master CHI clock source and the TMPR3922AU CHI module will slave to this external clock.
CHIDOUT	O	This pin is the CHI serial data output signal.
CHIDIN	I	This pin is the CHI serial data inaut signal.

- IO Pins

NAME	I/O	DESCRIPTION
IO[15:0]	I/O	These pins are general purpose input/output ports. Each port can be independently programmed as an input or output port. Each port can generate a separate positive and negative edge interrupt. Each port can also be independently programmed to use a 16 to 24ms debouncer.

- Reset Pins

NAME	I/O	DESCRIPTION
CPURES*	I	This pin is used to reset the CPU core. This pin should be connected to a switch for initiating a reset in the event that a software problem might hang the CPU core. The pin should also be pulled up to VSTANDBY† through an external pull-up resistor.
PON*	I	This pin serves as the Power On Reset signal for the TMPR3922AU. This signal must remain low when VSTANDBY is asserted until VSTANDBY is stable. Once VSTANDBY† is asserted, this signal should never go low unless all power is lost in the system.

† VSTANDBY : This signal provides power for the TMPR3922AU and other components in the system that must never lose power. This signal should always be asserted if there is either a good Main Backup Battery, or if a Battery Charger is plugged in.

- Power Supply Pins

NAME	I/O	DESCRIPTION
ONBUTN	I	This pin is used as the On Button for the system. Asserting this signal will cause PWRCS to set to indicate to the System Power Supply to turn power on to the system. PWRCS will not assert if the PWROK signal is low.
PWRCS	O	This pin is used as the chip select for the System Power Supply. When the system is off, the assertion of this signal will cause the System Power Supply to turn VCCDRAM†† and VCC3 on to power up the system. The Power Supply will latch SPI commands on the falling edge of PWRCS.
PWROK	I	This pin provides a status from the System Power Supply that there is a good source of power in the system. This signal typically will be asserted if there is a Battery Charger supplying current or if the Main Battery is good and the Battery Door is closed. If PWROK is low when the system is powered off, PWRCS will not assert as a result of the user pressing the ONBUTN or an interrupt attempting to wake up the system. If the device is on when the PWROK signal goes low, the software will immediately shut down the system since power is about to be lost. When PWROK goes low, there must be ample warning so that the software can shut down the system before power is actually lost.
PWRINT	I	This pin is used by the System Power Supply to alert the software that some status has changed in the System Power Supply and the software should read the status from the System Power Supply to find out what has changed. These will be low priority events, unlike the PWROK status, which is a high priority emergency case.
VCC3	I	This pin provides the status of the power supply for the ROM, TC35143F, system buffers, and other transient components in the system. This signal will be asserted by the System Power Supply when PWRCS is asserted, and will always be turned off when the system is powered down.

†† VCCDRAM : This signal provides power for the DRAM and/or SDRAM. This supply must be off when VSTANDBY is first asserted, and remain off until the system is powered up by the assertion of PWRCS. When the software subsequently powers down the system it may choose to keep this supply on to preserve the contents of memory.

- SIB Pins

NAME	I/O	DESCRIPTION
SIBDIN	I	This pin contains the input data shifted from TC35143F and/or external codec device.
SIBDOUT	O	This pin contains the output data shifted to TC35143F and/or external codec device.
SIBSCLK	O	This pin is the serial clock sent to TC35143F and/or external codec device. The programmable SIBSCLK rate is derived by dividing down from SIBMCLK.
SIBSYNC	O	This pin is the frame synchronization signal sent to TC35143F and/or external codec device. This frame sync is asserted for one clock cycle immediately before each frame starts and all devices connected to the SIB monitor SIBSYNC to determine when they should transmit or receive data.
SIBIRQ	I	This pin is a general purpose input port used for the SIB interrupt source from TC35143F. This interrupt source can be configured to generate an interrupt on either a positive and/or negative edge.
SIBMCLK	I/O	This pin is the master clock source for the SIB logic. This pin is available for use in one of two modes. First, SIBMCLK can be configured as a high-rate output master clock source required by certain external codec devices. In this mode all SIB clocks are synchronously slaved to the main TMPR3922AU system clock CLK2X. Conversely, SIBMCLK can be configured as an input slave clock source. In this mode, all SIB clocks are derived from an external SIBMCLK oscillator source, which is asynchronous with respect to CLK2X. Also, for this mode, SIBMCLK can still be optionally used as a high-rate master clock source required by certain external codec devices.

- SPI Pins

NAME	I/O	DESCRIPTION
SPICLK	I/O	This pin is used to clock data in and out of either the SPI master or slave device. This pin is the master clock source for the SPI logic. This pin is available for use in one of two modes. First, SPICLK can be configured as a master clock source required by certain external devices. In this mode all SPI clocks are synchronously slaved to the main TMPR3922AU system clock FREECLK. Conversely, SPICLK can be configured as an input slave clock source. In this mode, all SPI clocks are derived from an external oscillator source, which is asynchronous with respect to FREECLK.
SPIOUT	O	This pin contains the data that is shifted into the SPI slave device .
SPIIN	I	This pin contains the data that is shifted out of the SPI slave device.

- UART and SIR/FIR Pins

NAME	I/O	DESCRIPTION
TXD	O	This pin is the UART transmit signal from the UARTA module.
RXD	I	This pin is the UART receive signal to the UARTA module.
IROUT	O	This pin is the UART transmit signal from the UARTB module or the Consumer IR output signal if Consumer IR mode is enabled.
IRINA	I	This pin is the SIR receive signal to the IRDA(FIR/SIR) module.
IRINB	I	This pin is the FIR receive signal to the IRDA(FIR/SIR) module.
RXPWR	O	This pin is the receiver power output control signal to the external communication IR analog circuitry.
CARDET	I	This pin is the UART receive signal to the UARTB module or is the carrier detect input signal from the external communication IR analog circuitry if Consumer IR module is enabled.
FIROUT	O	This pin is the FIR/SIR transmit signal from the IRDA(FIR/SIR) module.

- Endian Pins

NAME	I/O	DESCRIPTION
ENDIAN	I	This pin is used to select the endian state of the TMPR3922AU. The "1" level input sets the endian state to the big endian, while the "0" level input to the little endian.

- Test Pins

NAME	I/O	DESCRIPTION
TESTAIU	I	This pin is used to define if the Boot ROM is 16 or 32 bits wide. If the TESTAIU pin is asserted during reset, the BIU will assume a 32-bit Boot ROM. The TESTAIU pin should remain static (either high or low).
TESTCPU	I	This pin is used for debugging purposes only. Then the TESTCPU should not be asserted.
TESTIN	I	This pin is used for debugging purposes only. Then the TESTIN should not be asserted.

- Spare Pins

NAME	I/O	DESCRIPTION
RESERVED	NC	These pins are reserved for future use and should be left unconnected.

- Power Supply Pins

NAME	I/O	DESCRIPTION
VDDH	V	These pins are the power pins for the TMPR3922AU.(+3.3V)
VDDL	V	These pins are the power pins for the TMPR3922AU.(+2.5V)
VDDLS	V	These pins are the power pins for the TMPR3922AU.(+2.5V) In the suspend mode these pins should be 0V.
VSS	G	These pins are the ground pins for the TMPR3922AU.
VDDP (for PLL)	V	This pin is the analog power pin for the TMPR3922AU. Keep away from other VDD.
VSSP (for PLL)	G	This pin is the analog ground pin for the TMPR3922AU. Keep away from other VSS.

4.3 PIN USAGE INFORMATION

This section contains tables summarizing various aspects of the pin usage for the TMPR3922AU. TABLE 4.3a lists the standard versus multi-function usage for each TMPR3922AU pin, if applicable. Those signal names shown in parentheses are test signals for debugging purposes only. The column showing the multi-function select signal and reset state indicates the internal control signal used to select the multi-function mode, as well as the default configuration of each multi-function pin during reset. The "Bus Arb State" column shows which pins are tri-stated whenever the DGRNT* signal is asserted in response to a DREQ*(external bus arbitration request).

TABLE 4.3a TMPR3922AU STANDARD and MULTI-FUNCTION PIN USAGE

TMPR3922AU pin	Standard Function (I = input, O = output)	Multi-function	Multi-function select (Reset State: 1 = multi-function mode selected; 0 = standard function & mode selected)	Bus Arb State
D[31:0]	D[31:0] (I/O)			Hi-Z
A[12:0]	A[12:0] (I/O)			
ALE	ALE (O)			Hi-Z
RD*	RD* (O)			Hi-Z
WE*	WE* (O)			Hi-Z
CAS0* (WE0*)	CAS0* (O)			Hi-Z
CAS1* (WE1*)	CAS1* (O)			Hi-Z
CAS2* (WE2*)	CAS2* (O)			Hi-Z
CAS3* (WE3*)	CAS3* (O)			Hi-Z
RAS0*	RAS0* (O)			Hi-Z
RAS1* (DCS1*)	RAS1* (O)			Hi-Z
DCS0*	DCS0* (O)			Hi-Z
DCKE	DCKE (O)			Hi-Z
DCLKIN	DCLKIN (I)			
DCLKOUT	DCLKOUT (O)			Hi-Z
DQMH	DQMH (O)			Hi-Z
DQML	DQML (O)			Hi-Z
DREQ*	DREQ* (I)	MIO[27]	MIOSEL[27] (0)	
DGRNT*	DGRNT* (O)	MIO[26]	MIOSEL[26] (0)	
SYSCLKIN	SYSCLKIN (I)			
SYSCLKOUT	SYSCLKOUT (O)			
C32KIN	C32KIN (I)			
C32KOUT	C32KOUT (O)			
C6MIN	C6MIN (I)			
C6MOUT	C6MOUT (O)			
C48MOUT	C48MOUT (O)			
BC32K	BC32K(O)	MIO[25]	MIOSEL[25] (1)	
BCLK	BCLK (O)			
PWRCS	PWRCS (O)			
PWRINT	PWRINT (I)			

TMPR3922AU pin	Standard Function (I = input, O = output)	Multi-function	Multi-function select (reset state: 1 = Multi-function Mode selected; 0 = Standard function & mode selected)	Bus Arb State
PWROK	PWROK (I)			
ONBUTN	ONBUTN (I)			
CPURES*	CPURES* (I)			
PON*	PON* (I)			
TXD	TXD (O)	MIO[24]	MIOSEL[24] (0)	
RXD	RXD (I)	MIO[23]	MIOSEL[23] (0)	
CS0*	CS0* (O)			Hi-Z
CS1*	CS1* (O)	MIO[22]	MIOSEL[22] (0)	
CS2*	CS2* (O)	MIO[21]	MIOSEL[21] (0)	
CS3*	CS3* (O)	MIO[20]	MIOSEL[20] (0)	
MCS0*	MCS0* (O)	MIO[19]	MIOSEL[19] (0)	
MCS1*	MCS1* (O)	MIO[18]	MIOSEL[18] (0)	
MCS0WAIT*	MCS0WAIT* (I)	MIO[0]	MIOSEL[0] (0)	
MCS1WAIT*	MCS1WAIT* (I)	MIO[1]	MIOSEL[1] (0)	
CHIFS	CHIFS (I/O)	MIO[31]	MIOSEL[31] (1)	
CHICLK	CHICLK (I/O)	MIO[30]	MIOSEL[30] (1)	
CHIDOUT	CHIDOUT (O)	MIO[29]	MIOSEL[29] (1)	
CHIDIN	CHIDIN (I)	MIO[28]	MIOSEL[28] (1)	
VCC3	VCC3 (I)			
IO15	IO15 (I/O)			
IO14	IO14 (I/O)			
IO13	IO13 (I/O)			
IO12	IO12 (I/O)			
IO11	IO11 (I/O)			
IO10	IO10 (I/O)			
IO9	IO9 (I/O)			
IO8	IO8 (I/O)			
IO7	IO7 (I/O)			
IO6	IO6 (I/O)			
IO5	IO5 (I/O)			
IO4	IO4 (I/O)			
IO3	IO3 (I/O)			
IO2	IO2 (I/O)			
IO1	IO1 (I/O)			
IO0	IO0 (I/O)			
SPICLK	SPICLK (I/O)	MIO[15]	MIOSEL[15] (0)	
SPIOUT	SPIOUT (O)	MIO[14]	MIOSEL[14] (0)	
SPIIN	SPIIN (I)	MIO[13]	MIOSEL[13] (0)	

TMPR3922AU pin	standard function (I = input, O = output)	multi-function	multi-function select (reset state: 1 = multi-function mode selected; 0 = standard function & mode selected)	Bus Arb State
SIBSYNC	SIBSYNC (O)			
SIBDOUT	SIBDOUT (O)			
SIBDIN	SIBDIN (I)			
SIBMCLK	SIBMCLK (I/O)	MIO[12]	MIOSEL[12] (0)	
SIBSCLK	SIBSCLK (O)			
SIBIRQ	SIBIRQ (I)			
RXPWR	RXPWR (O)	MIO[17]	MIOSEL[17] (1)	
CARDET	CARDET (I)			
IROUT	IROUT (O)	MIO[16]	MIOSEL[16] (1)	
IRINA	IRINA (I)			
IRINB	IRINB (I)			
FIROUT	FIROUT (O)			
TESTAIU	TESTAIU (I)			
TESTCPU	TESTCPU (I)			
TESTIN	TESTIN (I)			
CARDREG*	CARDREG*(O)	MIO[11]	MIOSEL[11] (1)	
CARDIOWR*	CARDIOWR* (O)	MIO[10]	MIOSEL[10] (1)	
CARDIORD*	CARDIORD* (O)	MIO[9]	MIOSEL[9] (1)	
CARD1CSL*	CARD1CSL* (O)	MIO[8]	MIOSEL[8] (1)	
CARD1SCH*	CARD1CSH* (O)	MIO[7]	MIOSEL[7] (1)	
CARD2CSL*	CARD2CSL* (O)	MIO[6]	MIOSEL[6] (1)	
CARD2CSH*	CARD2CSH* (O)	MIO[5]	MIOSEL[5] (1)	
CARD1WAIT*	CARD1WAIT* (I)	MIO[4]	MIOSEL[4] (1)	
CARD2WAIT*	CARD2WAIT* (I)	MIO[3]	MIOSEL[3] (1)	
CARDDIR*	CARDDIR* (O)	MIO[2]	MIOSEL[2] (1)	
ENDIAN	ENDIAN (I)			
VDDH	+3.3V			
VDDL	+2.5V			
VDDLS	+ 2.5 V / GND			
VDDP	+2.5V			
VSS	GND			
VSSP	GND			

TABLE 4.3b lists various power-down states and conditions for each TMPR3922AU pin. The "Power-Down Control" column shows the conditions which trigger a power-down for each respective pin. This column also shows the reset state for each of these conditions.

The "PON* state" column defines the state of each pin at power-on reset (PON*). This condition is defined as initial power up of the TMPR3922AU, whereby the TMPR3922AU is initialized and the TMPR3922AU pins are reset to the state shown in the table. This state is entered after power is applied for the very first time (VSTANDBY is turned on but VCC3 is still turned off).

The "1st-time power-up state" column defines the state of each pin after power-up mode (RUNNING STATE) is executed for the first time. This mode is defined as VCC3 applied to the entire system and is initiated by the user pressing the ONBUTN while in the power-on reset (PON*) state. Note that the defined state of various pins for 1st-time power-up may depend on the configuration of external devices attached to these pins. After 1st-time power-up, the software could change the state of various pins to be different from those shown in the table. Thereafter, subsequent transitions from SLEEP STATE to RUNNING STATE might result in different states for these pins.

The "power-down state" column defines the state of each pin during power-down mode (SLEEP STATE). This mode is defined as VCC3 turned off to the entire system, except for the TMPR3922AU (RTC and interrupts alive) and any persistent memory.

TABLE 4.3b TMPR3922AU POWER-DOWN PIN USAGE

TMPR3922AU pin	Power-Down Control powerdown = (vccon & vcc3)* (reset state)	PON* state	1st time power-up state	power-down state
D[31:0]	MEMPOWERDOWN	LOW	LOW	LOW
A[12:0]	MEMPOWERDOWN	LOW	LOW	LOW
ALE		LOW	LOW	LOW
RD*	POWERDOWN	LOW	HI	LOW
WE*	MEMPOWERDOWN	LOW	LOW	LOW
CAS0* (WE0*)	MEMPOWERDOWN	LOW	LOW	LOW
CAS1* (WE1*)	MEMPOWERDOWN	LOW	LOW	LOW
CAS2* (WE2*)	MEMPOWERDOWN	LOW	LOW	LOW
CAS3* (WE3*)	MEMPOWERDOWN	LOW	LOW	LOW
RAS0*	MEMPOWERDOWN	LOW	LOW	LOW
RAS1* (DCS1*)	MEMPOWERDOWN	LOW	LOW	LOW
DCS0*	MEMPOWERDOWN	LOW	LOW	LOW
DCKE	MEMPOWERDOWN	LOW	LOW	LOW
DCLKIN				
DCLKOUT	MEMPOWERDOWN	LOW	LOW	LOW
DQMH	MEMPOWERDOWN	LOW	LOW	LOW
DQML	MEMPOWERDOWN	LOW	LOW	LOW
DREQ*	POWERDOWN & MIOPD[27] (1)	PULL-DOWN	IN	SELECTABLE
DGRNT*	POWERDOWN & MIOPD[26] (0)	LOW	HI	SELECTABLE
SYSCLKIN	POWERDOWN	OSC OFF	OSC ON	OSC OFF
SYSCLKOUT	POWERDOWN	OSC OFF	OSC ON	OSC OFF
C32KIN		OSC ON	OSC ON	OSC ON
C32KOUT		OSC ON	OSC ON	OSC ON
C6MIN	POWERDOWN	OSC OFF	OSC ON	OSC OFF
C6MOUT	POWERDOWN	OSC OFF	OSC ON	OSC OFF
C48MOUT	POWERDOWN	LOW	LOW	LOW
BC32K	POWERDOWN & MIOPD[25] (1)	PULL-DOWN	IN	SELECTABLE
BCLK	POWERDOWN	LOW	LOW	LOW

TMPR3922AU pin	Power-Down Control powerdown = (vccon & vcc3)* (reset state)	PON* state	1st time power-up state	power-down state
PWRCS		LOW	HI	LOW
PWRINT				
PWROK				
ONBUTN				
CPURES*				
PON*				
TXD	POWERDOWN & MIOPD[24] (0)	LOW	LOW	SELECTABLE
RXD	POWERDOWN & MIOPD[23] (1)	PULL-DOWN	IN	SELECTABLE
CS0*	POWERDOWN	PULL-DOWN	HI	PULL-DOWN
CS1*	POWERDOWN & MIOPD[22] (1)	PULL-DOWN	HI	SELECTABLE
CS2*	POWERDOWN & MIOPD[21] (1)	PULL-DOWN	HI	SELECTABLE
CS3*	POWERDOWN & MIOPD[20] (1)	PULL-DOWN	HI	SELECTABLE
MCS0*	POWERDOWN & MIOPD[19] (0)	IN	IN	SELECTABLE
MCS1*	POWERDOWN & MIOPD[18] (0)	IN	IN	SELECTABLE
MCS0WAIT*	POWERDOWN & MIOPD[1] (0)	IN	IN	SELECTABLE
MCS1WAIT*	POWERDOWN & MIOPD[0] (0)	IN	IN	SELECTABLE
CHIFS	POWERDOWN & MIOPD[31] (1)	PULL-DOWN	IN	SELECTABLE
CHICLK	POWERDOWN & MIOPD[30] (1)	PULL-DOWN	IN	SELECTABLE
CHIDOUT	POWERDOWN & MIOPD[29] (1)	PULL-DOWN	IN	SELECTABLE
CHIDIN	POWERDOWN & MIOPD[28] (1)	PULL-DOWN	IN	SELECTABLE
VCC3	POWERDOWN	PULL-DOWN		PULL-DOWN
IO15	POWERDOWN & IOPD[15] (1)	POLL-DOWN	IN	SELECATBLE
IO14	POWERDOWN & IOPD[14] (1)	PULL-DOWN	IN	SELECATBLE
IO13	POWERDOWN & IOPD[13] (1)	PULL-DOWN	IN	SELECATBLE
IO12	POWERDOWN & IOPD[12] (1)	PULL-DOWN	IN	SELECATBLE
IO11	POWERDOWN & IOPD[11] (1)	PULL-DOWN	IN	SELECTABLE
IO10	POWERDOWN & IOPD[10] (1)	PULL-DOWN	IN	SELECTABLE
IO9	POWERDOWN & IOPD[9] (1)	PULL-DOWN	IN	SELECTABLE
IO8	POWERDOWN & IOPD[8] (1)	PULL-DOWN	IN	SELECTABLE
IO7	POWERDOWN & IOPD[7] (1)	PULL-DOWN	IN	SELECTABLE
IO6	POWERDOWN & IOPD[6] (1)	PULL-DOWN	IN	SELECTABLE
IO5	POWERDOWN & IOPD[5] (1)	PULL-DOWN	IN	SELECTABLE
IO4	POWERDOWN & IOPD[4] (1)	PULL-DOWN	IN	SELECTABLE
IO3	POWERDOWN & IOPD[3] (1)	PULL-DOWN	IN	SELECTABLE
IO2	POWERDOWN & IOPD[2] (1)	PULL-DOWN	IN	SELECTABLE
IO1	POWERDOWN & IOPD[1] (1)	PULL-DOWN	IN	SELECTABLE
IO0	POWERDOWN & IOPD[0] (1)	PULL-DOWN	IN	SELECTABLE
SPICLK	POWERDOWN & MIOPD[15] (0)	LOW	LOW	SELECTABLE
SPIOUT	POWERDOWN & MIOPD[14] (0)	LOW	LOW	SELECTABLE
SPIIN	POWERDOWN & MIOPD[13] (1)	PULL-DOWN		SELECTABLE

TMPR3922AU pin	Power-Down Control powerdown = (vccon & vcc3)* (reset state)	PON* state	1st time power-up state	power-down state
SIBSYNC	POWERDOWN	LOW	LOW	LOW
SIBDOUT	POWERDOWN	LOW	LOW	LOW
SIBDIN	POWERDOWN	PULL-DOWN		PULL-DOWN
SIBMCLK	POWERDOWN & MIOPD[12] (1)	PULL-DOWN	IN	SELECTABLE
SIBSCLK	POWERDOWN	LOW	LOW	LOW
SIBIRQ	POWERDOWN	PULL-DOWN		PULL-DOWN
RXPWR	POWERDOWN & MIOPD[17] (0)	PULL-DOWN	IN	SELECTABLE
IROUT	POWERDOWN & MIOPD[16] (0)	PULL-DOWN	IN	SELECTABLE
CARDET	POWERDOWN	PULL-DOWN	X	PULL-DOWN
IRINA				
IRINB				
FIROUT	POWERDOWN	LOW	LOW	LOW
TESTAIU				
TESTCPU				
TESTIN				
CARDREG*	POWERDOWN & MIOPD[11] (1)	PULL-DOWN	IN	SELECTABLE
CARDIOWR*	POWERDOWN & MIOPD[10] (1)	PULL-DOWN	IN	SELECTABLE
CARDIORD*	POWERDOWN & MIOPD[9] (1)	PULL-DOWN	IN	SELECTABLE
CARD1CSL*	POWERDOWN & MIOPD[8] (1)	PULL-DOWN	IN	SELECTABLE
CARD1CSH*	POWERDOWN & MIOPD[7] (1)	PULL-DOWN	IN	SELECTABLE
CARD2CSL*	POWERDOWN & MIOPD[6] (1)	PULL-DOWN	IN	SELECTABLE
CARD2CSH*	POWERDOWN & MIOPD[5] (1)	PULL-DOWN	IN	SELECTABLE
CARD1WAIT*	POWERDOWN & MIOPD[4] (1)	PULL-DOWN	IN	SELECTABLE
CARD2WAIT*	POWERDOWN & MIOPD[3] (1)	PULL-DOWN	IN	SELECTABLE
CARDDIR*	POWERDOWN & MIOPD[2] (1)	PULL-DOWN	IN	SELECTABLE
ENDIAN				
VDDH				
VDDL				
VDDLS				
VDDP				
VSS				
VSSP				

5. FUNCTION SPECIFICATIONS

5.1 OUTLINE

The TMPR3922AU consists of PDA system support logic, integrated with the TX3920 Processor Core designed by Toshiba. For details of the system support logic and the TX3920 processor Core, refer to the TMPR3922AU User's manual and TX39 family user's manual, respectively.

5.2 TX3920 PROCESSOR CORE

The TX3920 processor core is a Toshiba-developed microprocessor core based on the R3000A RISC architecture developed by The MIPS Group, a division of Silicon Graphics, Inc. of the United States.

5.2.1 INSTRUCTIONS

All TX3920 Processor Core instructions are 32-bit instructions. Apart from some coprocessor instructions, the instructions are upwardly compatible with the R3000A. The TX3920 Processor Core instructions can be classified into six types.

- Load and store instructions

  Transfer data between memory and general-purpose registers.

- Computational instructions

  These include arithmetic, logical, shift, multiply, divide, and multiply-add instructions. The multiply-add instructions are extensions to the R3000A. The multiply instructions can also be used as three-operand instructions.

- Special instructions

  Used for system call or break point.

- Jump and branch instructions

  Change the control flow of a program. The Branch-Likely instruction is provided as an extension to the R3000A.

- Coprocessor instructions

  Perform operations for coprocessors. The R3000A LWCz and SWCz instructions are reserved instructions in the TX3920 Processor Core. Attempting execution generates a reserved instruction exception. Note that the COPz, CTCz and MTCz instructions are no-operation instructions, the CFCz and MFCz instructions load undefined data to general purpose registers (rt) in the TMPR3922AU.

- System control coprocessor instructions

  Perform operations on the CP0 registers to manipulate the memory management and exception handling functions of the processor.

5.2.2 REGISTERS

The TX3920 Processor Core has following registers.

- 32 general purpose registers (32-bit)
- HI/LO registers

  Hold the result of multiply and divide operation
- PC (Program Counter)
- Cause register

  Indicates the nature of the most recent exception
- EPC (Exception Program Counter) register

  Holds the program counter at the time the exception occurred, indicating the address where processing is to resume after the exception processing is completed.
- Status register

  Holds the operating mode status (user mode or kernel mode), interrupt masking status, diagnosis status and other such information.
- BadVAddr (Bad Virtual Address) register

  Holds the most recent virtual address for which a virtual address translation error occurred.
- PRId register

  Shows the revision number of the TX3920 Processor Core. (PRId:0x00002230)
- Cache register

  Controls the instruction cache (reserved) and the data cache auto-lock bits.
- Config register

  Some configuration options.
- Context register
- Entry HI/LO register
- Index register
- Tag LO register
- Random register

  TLB Random index.
- Page Mask register

  Hold a comparison mask that sets the variable page sige for each TLB entry.
- Wired register

  TLB Wired boundary.
- Debug register

  Control software debug exception.
- DEPC

  Program counter for software debug exception.

5.2.3 MEMORY MANAGEMENT

The TX3920 Processor Core has a 4G-byte memory address space. The 4G-byte memory space consists of a 2G-byte user area and a 2G-byte kernel area. The kernel area contains a cache area and an uncache area.The TX3920 Processor Core provides a full-featured memory management unit (MMU) utilizing an on-chip Translation Lookaside Buffer (TLB). The on-chip TLB majur characteristics are :

- 64×64-bit wide entries
- 4K / 16K / 64K / 256K / 1M / 4M page size
- fully associative
- 2 entry micro TLB for instruction address translation
- instruction address translation accesses full TLB after micro-TLB miss
- data address translation accesses full TLB

5.2.4 PIPELINE

The TX3920 Processor Core pipeline consists of five stages. The pipeline configuration enables the TX3920 Processor Core to execute nearly all instructions in one clock.

5.2.5 CACHE

The TMPR3922AU incorporates a 16K-byte instruction cache and an 8K-byte data cache. The instruction cache uses two-way set-associative mapping with a block size of 16 bytes. The data cache uses two-way set-associative mapping with a block size of four bytes. Both data and Instruction cache have a lock function that locks data in one direction. Either copy-back or write-through method is used to write data back to memory.

5.2.6 DSP FUNCTION

The TX3920 Processor Core has a high-speed multiplier/accumulator and supports 32-bit × 32-bit multiplier operations, with 64-bit accumulator in one cycle.

5.3 PERIPHERAL FUNCTIONS

5.3.1 CLOCK GENERATOR

The TMPR3922AU uses an internal PLL and an external crystal oscillator to generate a clock with 16 times the input clock frequency. The PLL oscillation can be halted externally to reduce power dissipation.

5.3.2 WRITE BUFFER

The TMPR3922AU incorporates a four-stage write buffer.

5.3.3 BUS INTERFACE UNIT (BIU) MODULE

The TMPR3922AU has a Bus Interface Unit with the following features.

- supports 2 Banks of SDRAM and/or DRAM(EDO)
  - 16-bit or 32-bit SDRAM configuration
  - 16-bit or 32-bit DRAM(EDO) configuration
  - 4 Mbit, 16 Mbit and 64 Mbit parts supported
  - page mode reads and writes supported
  - independent refresh counters for each bank
  - self refreshing parts supported to retain memory when system is powered down
- 4 general purpose chip selects (CS3*-CS0*)
  - 16-bit or 32-bit ports
  - programmable wait states
  - read page mode
- 2 general purpose chip selects (MCS1*- MCS0*)
  - 16-bit or 32-bit ports
  - programmable wait states
  - read page mode
  - WAIT signal supported
- 2 full PCMCIA slots
  - 8-bit or 16-bit ports
  - IORD and IOWR provided to support I/O cards
  - WAIT signal supported

5.3.4 SYSTEM INTERFACE UNIT (SIU) MODULE

The TMPR3922AU has a System Interface Unit with the following features.

- multi-channel 32-bit DMA controller
- independent DMA controller for SIB to/from TC35143F audio/telecom codecs, high-speed serial port, IRDA, UART, and general purpose UART
- address decoding for the internal registers

5.3.5 CLOCK MODULE

The TMPR3922AU has a Clock module with the following features.

- The TMPR3922AU supports system-wide single crystal configuration, besides the 32 kHz RTC X'tal (reduces cost, power, and board space)
- common crystal rate divided to generate clock for CPU, sound, telecom, UARTs, etc.
- independent enabling or disabling of individual clocks under software control, for power management

5.3.6 CONCENTRATION HIGHWAY INTERFACE (CHI) MODULE

The TMPR3922AU has a CHI module with the following features.

- high-speed serial Concentration Highway Interface (CHI) contains logic for interfacing to external full-duplex serial time-division-multiplexed (TDM) communication peripherals
- supports ISDN line interface chips and other PCM/TDM serial devices
- CHI interface is programmable (number of channels, frame rate, bit rate, etc.) to provide support for a variety of formats
- supports data rates up to 4.096 Mbps
- independent DMA support for CHI receive and transmit

5.3.7 INTERRUPT MODULE

The TMPR3922AU has an Interrupt module with the following features.

- contains logic for individually enabling, reading, and clearing all TMPR3922AU interrupt sources
- interrupts generated from internal TMPR3922AU modules or from edge transitions on external signal pins

5.3.8 IO MODULE

The TMPR3922AU has an IO module with the following features.

- contains support for reading and writing the 16 bi-directional general purpose IO pins and the 32 bi-directional multi-function IO pins
- each IO port can generate a separate positive and negative edge interrupt
- independently configurable IO ports allow the TMPR3922AU to support a flexible and wide range of system applications and configurations

5.3.9 IR MODULE

The TMPR3922AU has an IR module with the following features.

- IR consumer mode
  - allows control of consumer electronic devices such as stereos, TVs, VCRs, etc.
  - programmable pulse parameters
  - external analog LED circuitry
- IRDA communication mode
  - IrDA 1.0 mode with filter is supported(BOF and EOF are detected by hardware and the bit pattern which data translation is necessay is detected and translated by hardware.)
  - Also IrDA 1.1 compliance(2.4/9.6/19.2/38.4/57.6/115.2 kbps are available)
  - 1.152 Mbps NRZ supported
  - 4 Mbps 4ppm/single plus supported(512 kbps and 4 Mbps with double pluse are not supported)
  - CRC generation/check supported
  - Address filter mode supported
  - Powe down mode(Power down register controls FIR clock to reduce power)
  - supported by the UART module within the TMPR3922AU
  - external analog receiver preamp and LED circuitry
  - data rate = up to 115 kbps at 1 meter
- IR FSK communication mode
  - supported by the UART module within the TMPR3922AU
  - external analog IR chip(s) perform frequency modulation to generate the desired IR communication mode protocol
  - data rate = up to 36000 bps at 3 meters
- carrier detect state machine
  - periodically enables IR receiver to check if a valid carrier is present

5.3.10 POWER MODULE

The TMPR3922AU has a Power module with the following features.

- power-down modes for individual internal peripheral modules
- serial (SPI port) power supply control interface supported
- power management state machine has 3 states: RUNNING, DOZING and SLEEP

5.3.11 SERIAL INTERCONNECT BUS (SIB) MODULE

The TMPR3922AU has a SIB module with the following features.

- The TMPR3922AU contains holding and shift registers to support the serial interface to the TC35143F codec devices
- interface compatible with slave mode 3 of the Crystal CS4216 codec
- synchronous, frame-based protocol
- The TMPR3922AU always master source of clock and frame frequency and phase; programmable clock frequency
- each SIB frame consists of 128 clock cycles, further divided into 2 subframes or words of 64 bits each (supports up to 2 devices simultaneously)
- independent DMA support for audio receive and transmit, telecom receive and transmit
- supports 8-bit or 16-bit mono telecom formats
- supports 8-bit or 16-bit mono or stereo audio formats
- independently programmable audio and telecom sample rates
- CPU read/write registers for subframe control and status

5.3.12 SERIAL PERIPHERAL INTERFACE (SPI) MODULE

The TMPR3922AU has an SPI module with the following features.

- provides interface to SPI peripherals and devices
- full-duplex, synchronous serial data transfers (data in, data out, and clock signals)
- The TMPR3922AU supplies dedicated chip select and interrupt for an SPI interface serial power supply
- 8-bit or 16-bit data word lengths for the SPI interface
- programmable SPI baud rate

5.3.13 TIMER MODULE

The TMPR3922AU has a Timer module with the following features.

- Real Time Clock (RTC) and Timer
- 43-bit counter (30.517 μs granularity); maximum uninterrupted time = 3104 days
- 43-bit alarm register (30.517 μs granularity)
- 16-bit periodic timer (0.868 μs granularity); maximum timeout = 56.8 ms
- interrupts on alarm, timer, and prior to RTC roll-over

5.3.14 UART MODULE

The TMPR3922AU has a UART module with the following features.

- 2 independent full-duplex UARTs
- programmable baud rate generator
- UARTA port used for general purpose serial control interface
- UARTB port used for serial control interface to external IR module
- UARTA and UARTB DMA support for receive and transmit

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0 V (GND)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DDH}	V_{SS}-0.5 to 4.5	V
	V_{DDL}, V_{DDLS} V_{DDP}	V_{SS}-0.5 to 3.5	V
Input voltage	V_{IN}	V_{SS} - 0.5 to V_{DDH} + 0.5	V
Storage temperature	T_{STG}	- 55 to 125	°C
Maximum dissipation (Ta = 70°C)	P_D	1	W

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

6.2 RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0 V (GND)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power Supply voltage	V_{DDH}		3.0	3.3	3.6	V
	V_{DDL},V_{DDLS} V_{DDP}		2.5	2.7	2.9	V
Operating temperature	T_{OPR}		0	–	70	°C

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified.
If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating Conditions for the device are always adhered to.

6.3 DC CHARACTERISTICS

(T_a = 0°C~70°C, V_{DDH} = 3.3V±0.3V,V_{DDL} and V_{DDLS} = 2.7V±0.2V)

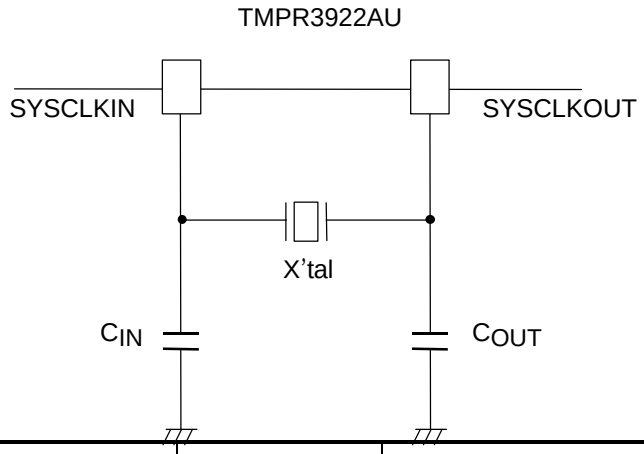
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating current	I_{DD}	V_{IN} = V_{DDH} or V_{SS} V_{DDH} = MAX V_{DDL} = V_{DDLS} =MAX I_{OH} = I_{OL} = 0 mA fin(6)= 9MHz	–	150	–	mA
Static current	I_{DDS}	V_{IN} = V_{DDH} or V_{SS} V_{DDH} = 2.7 3.3V V_{DDL} = 2.7V V_{DDLS} = 0V I_{OH} = I_{OL} = 0 mA SLEEP mode & RTC stop mode	–	50	100	mA
	I_{DDS}	V_{IN} = V_{DDH} or V_{SS} V_{DDH} = 2.7 3.3V V_{DDL} = 2.7V V_{DDLS} = 0V I_{OH} = I_{OL} = 0 mA SLEEP mode & RTC Running mode	–	60	110	mA
Input Leakage current	I_{IN}	V_{IN} = V_{DDH} or V_{SS}	-10	–	10	mA
Input voltage (1)	V_{IH1}	V_{DDH} = 3.6V	V_{DD}×0.8	–	V_{DD}+0.3	V
	V_{IL1}	V_{DDH} = 3.0V	-0.3	–	V_{DD}×0.2	V
Input voltage (2)	V_{IH2}	V_{DDH} = 3.6V	2.4	–	V_{DD}+0.3	V
	V_{IL2}	V_{DDH} = 3.0V	-0.3	–	0.6	V
Output voltage (3)	V_{OH1}	V_{DDH} = 3.0V, I_{OH} = -4mA	V_{DD}-0.6	–	–	V
	V_{OL1}	V_{DDH} = 3.0V, I_{OL} = -4mA	–	–	V_{DD}+0.4	V
Output voltage (4)	V_{OH2}	V_{DDH} = 3.0V, I_{OH} = -8mA	V_{DD}-0.6	–	–	V
	V_{OL2}	V_{DDH} = 3.0V, I_{OL} = -8mA	–	–	V_{DD}+0.4	V
Output voltage (5)	V_{OH3}	V_{DDH} = 3.0V, I_{OH} = -16mA	V_{DD}-0.6	–	–	V
	V_{OL3}	V_{DDH} = 3.0V, I_{OL} = -16mA	–	–	V_{DD}+0.4	V
Input current (Pull-down resister)	I_{IHP}	V_{DDH} = MAX VIN = V_{DDH}	20	–	120	mA

(1) SYSCLKIN, C32KIN, C6MIN
(2) Other inputs
(3) D[31:0], RAS[1:0]*, DCS0*, DCKE*, DQMH, DQML, DGRNT*, C48MOUT, BCLK, BC32K, PWRCS, TXD, CS[3:O]*, CHIFS, CHICLK, CHIDOUT, IO[15:0], SPICLK, SPIOUT, SIBSYNC, SIBDOUT, SIBMCLK, SIBSCLK, RXPWR, IROUT, CARDDIR*, MCS[1:0] *, FIROUT
(4) A[12:0], ALE, RD*, WE*, CAS[3:O]*, CARDREG*, CARDIORD*, CARDIOWR*, CARD1CSL*, CARD1CSH*, CARD2CSL*, CARD2CSH*
(5) DCLKOUT
(6) Crystal Oscillator frequency of SYSCLK = 9MHz

6.4 CRYSTAL OSCILLATOR CHARACTERISTICS

6.4.1 CRYSTAL OSCILLATOR CONDITIONS

(1) 10MHz CRYSTAL

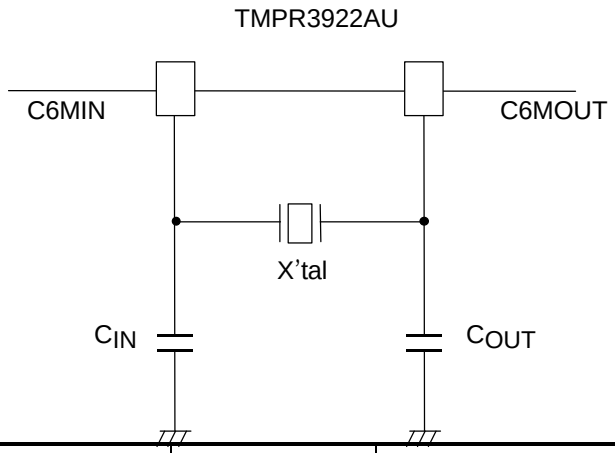


Parameter	Symbol	Recommended value		Unit
		MIN.	MAX.	
Crystal Oscillator frequency	f_{IN}	8	12	MHz
External capacitors	C_{IN},C_{OUT}	10	33	pF

Please note that there are some consideration on the location of the external crystal as follows.

1. Please place the crystal as close to the TMPR3922AU as possible.
2. Please place the crystal as far from data bus lines as possible.
3. Please surround the crystal area with GND.

(2) 6MHz CRYSTAL

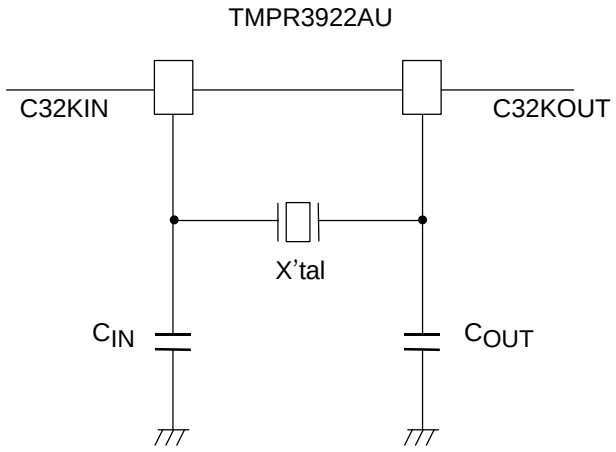


Parameter	Symbol	Recommended value		Unit
		MIN.	MAX.	
External capacitors	C_{IN},C_{OUT}	10	33	pF

Please note that there are some consideration on the location of the external crystal as follows.

1. Please place the crystal as close to The TMPR3922AU as possible.
2. Please place the crystal as far from data bus lines as possible.
3. Please surround the crystal area with GND.

(3) 32kHz CRYSTAL



Parameter	Symbol	Recommended value		Unit
		MIN.	MAX.	
External capacitors	C_{IN},C_{OUT}	10	33	pF

Please note that there are some consideration on the location of the external crystal as follows.

1. Please place the crystal as close to The TMPR3922AU as possible.
2. Please place the crystal as far from data bus lines as possible.
3. Please surround the crystal area with GND.

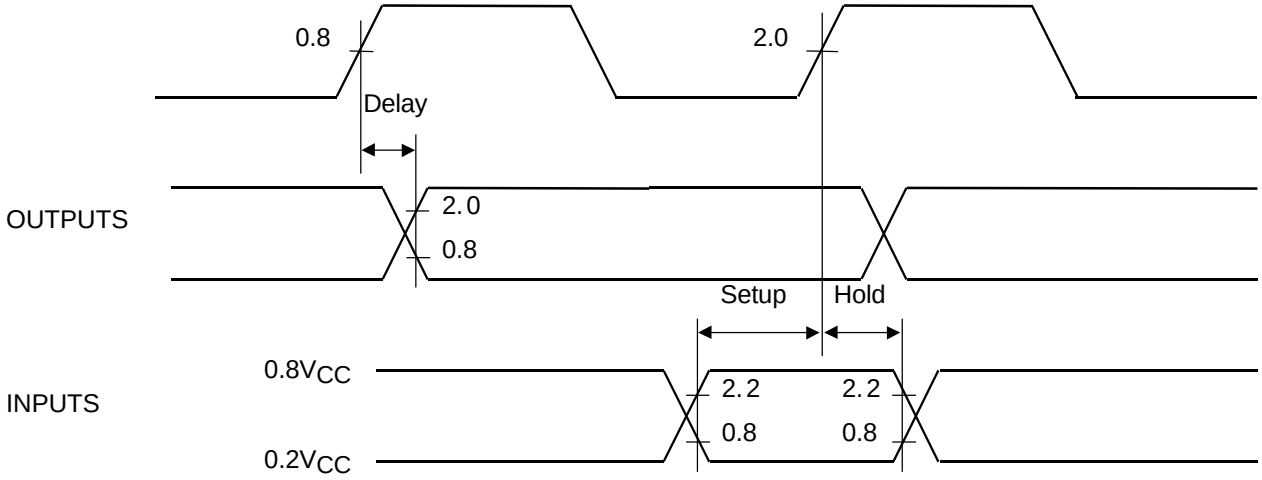
6.4.2 ELECTRICAL SPECIFICATIONS

(V_{SS} = 0V, V_{DDH} = 3.3V, V_{DDL} = V_{DDLS} = 2.5V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Crystal stabilization time 10MHz	$T_{STA-10M}$	f = 8MHz~12MHz Cin = Cout = 10pF~33pF	–	–	10	ms
Crystal stabilization time 6MHz	T_{STA-6M}	f = 6.0MHz Cin = Cout = 10pF~33pF	–	–	10	ms
Crystal stabilization time 32kHz	$T_{STA-32k}$	f = 32kHz Cin = Cout = 10pF~33pF	–	–	2	s

6.5 TMPR3922AU TIMING

6.5.1 DEFINITION OF AC SPECIFICATION



6.6 AC CHARACTERISTICS

The following operating conditions apply to all values specified in this section.

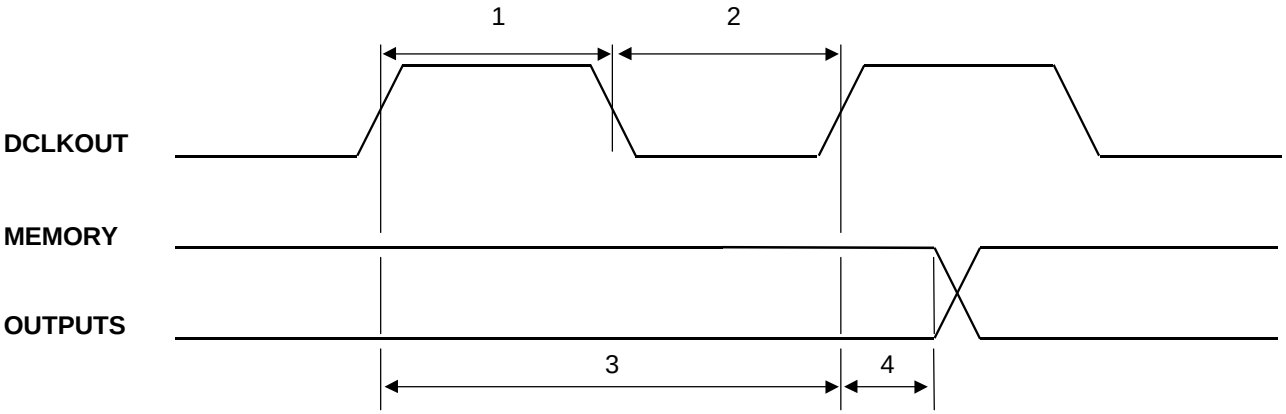
T_a = 0~70ºC, V_{DDH} = 3.3±0.3V, V_{DDL} = V_{DDLS} =2.7±0.2V, External Capacitance = 40pF

<Memory Interface>

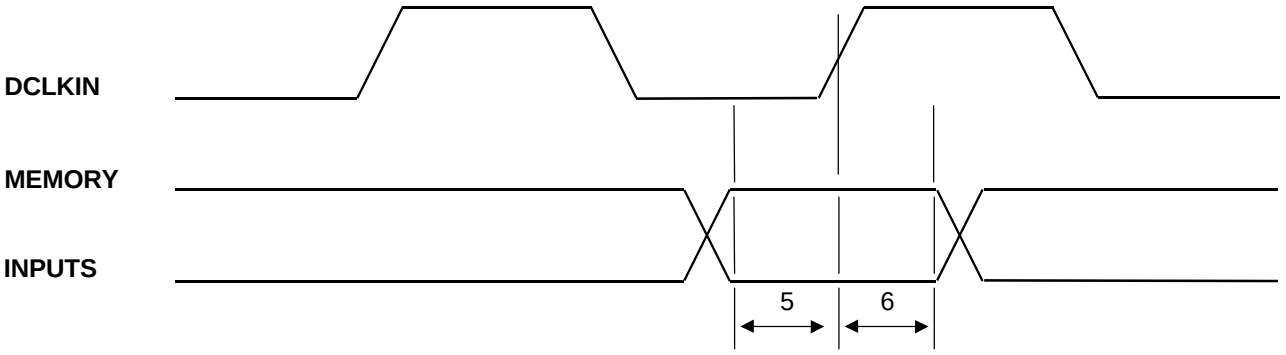
Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	DCLKOUT high time	–	6.1	–	ns
2	DCLKOUT low time	–	6.1	–	ns
3	DCLKOUT period	–	15.4	–	ns
4	Delay DCLKOUT to ALE	Rising	–	4	ns
4	Delay DCLKOUT to ALE	Falling	–	4	ns

<Memory Interface>

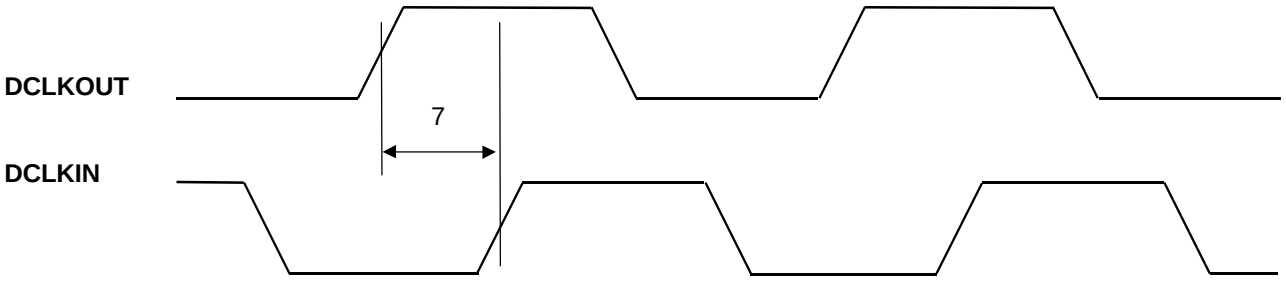
Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
4	Delay DCLKOUT to A[12:0]	–	–	8	ns
4	Delay DCLKOUT to D[31:16]	–	1.5	8	ns
4	Delay DCLKOUT to CS3-0*	Rising	–	10	ns
4	Delay DCLKOUT to CS3-0*	Falling	–	10	ns
4	Delay DCLKOUT to RD*	Rising	–	8	ns
4	Delay DCLKOUT to RD*	Falling	–	8	ns
4	Delay DCLKOUT to WE*	Rising	–	8	ns
4	Delay DCLKOUT to WE*	Falling	–	8	ns
4	Delay DCLKOUT to CAS3-0*	Rising	1.5	8	ns
4	Delay DCLKOUT to CAS3-0*	Falling	1.5	8	ns
4	Delay DCLKOUT to CARDxCSx*	Rising	–	10	ns
4	Delay DCLKOUT to CARDxCSx*	Falling	–	10	ns
4	Delay DCLKOUT to CARDDIR*	Rising	–	10	ns
4	Delay DCLKOUT to CARDDIR*	Falling	–	10	ns
4	Delay DCLKOUT to CARDREG*	Rising	–	10	ns
4	Delay DCLKOUT to CARDREG*	Fatting	–	10	ns
4	Delay DCLKOUT to CARDIORD*	Rising	–	10	ns
4	Delay DCLKOUT to CARDIORD*	Falling	–	10	ns
4	Delay DCLKOUT to CARDIOWR*	Rising	–	10	ns
4	Delay DCLKOUT to CARDIOWR*	Falling	–	10	ns
4	Delay DCLKOUT to RAS0*	Rising	–	8	ns
4	Delay DCLKOUT to RAS0*	Falling	–	8	ns
4	Delay DCLKOUT to RAS1*	Rising	1.5	8	ns
4	Delay DCLKOUT to RAS1*	Falling	1.5	8	ns
4	Delay DCLKOUT to DQMH/L	Rising	1.5	8	ns
4	Delay DCLKOUT to DQMH/L	Falling	1.5	8	ns
4	Delay DCLKOUT to DCS0*	Rising	1.5	8	ns
4	Delay DCLKOUT to DCS0*	Falling	1.5	8	ns
4	Delay DCLKOUT to DCKE	Rising	1.5	8	ns
4	Delay DCLKOUT to DCKE	Falling	1.5	8	ns
4	Delay DCLKOUT to MCS1-0*	Rising	–	10	ns
4	Delay DCLKOUT to MCS1-0*	Falling	–	10	ns
5	D[31 : 16] to DCLKIN Setup time	–	1	–	ns
6	D[31 : 16] to DCLKIN Hold time	–	2	–	ns
5	D[15:0] to DCLKIN Setup time	–	0	–	ns
6	D[15:0] to DCLKIN Hold time	–	2.5	–	ns
7	DCLKOUT to DCLKIN Board Delay time	–	0	3	ns



Memory Output and Clock Timing



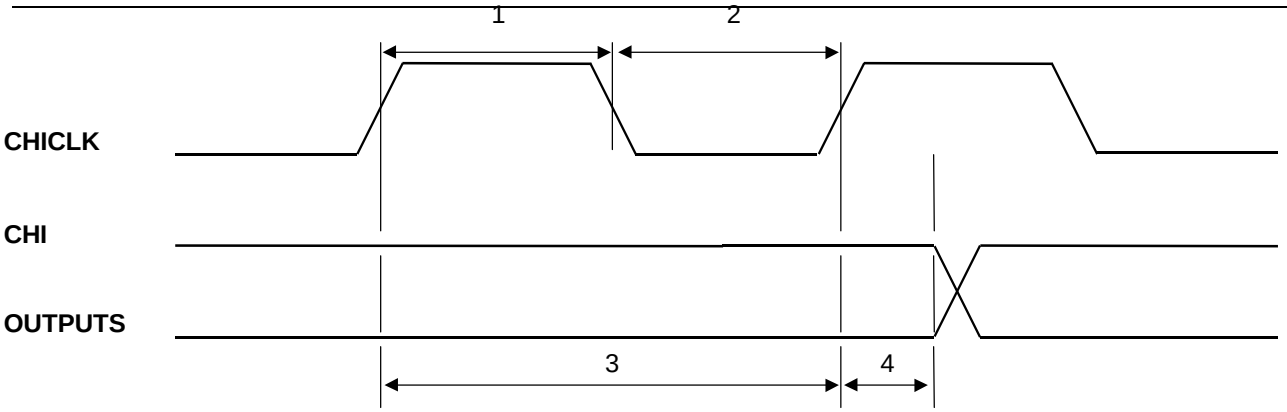
Memory Input Timing



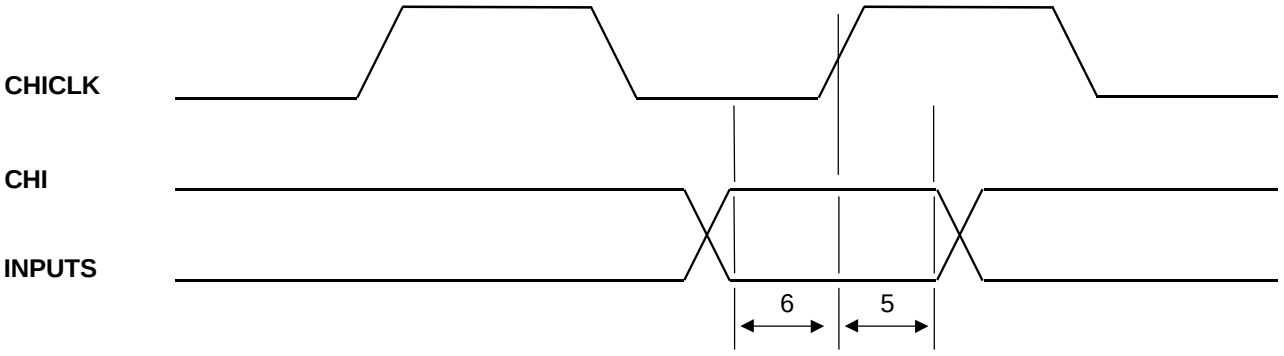
DCLKOUT to DCLKIN

<CHI>

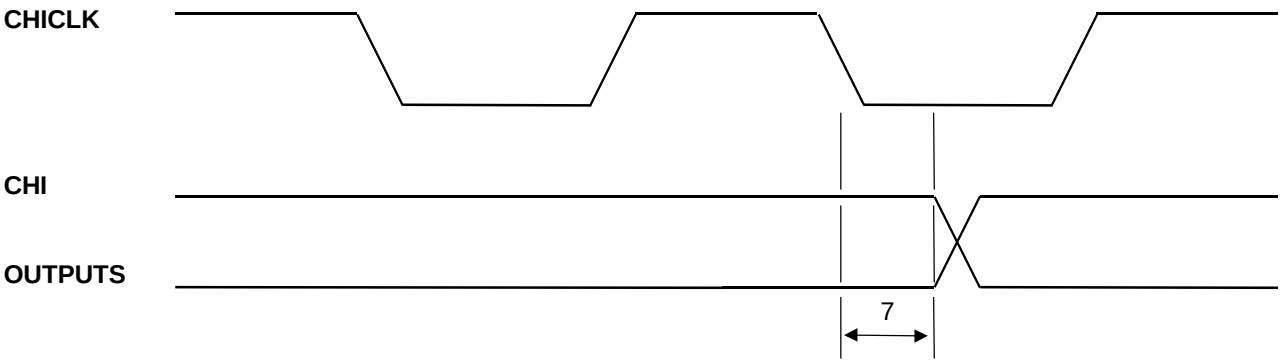
Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	CHICLK high time	–	100	–	ns
2	CHICLK low time	–	100	–	ns
3	CHICLK period	–	225	–	ns
4	Delay CHICLK Rising to CHIDOUT(Master)	Rising	–	10	ns
4	Delay CHICLK Rising to CHIDOUT(Master)	Falling	–	10	ns
7	Delay CHICLK Falling to CHIDOUT(Master)	Rising	–	10	ns
7	Delay CHICLK Falling to CHIDOUT(Master)	Falling	–	10	ns
4	Delay CHICLK Rising to CHIFS(Master)	Rising	–	10	ns
4	Delay CHICLK Rising to CHIFS(Master)	Falling	–	10	ns
7	Delay CHICLK Falling to CHIFS(Master)	Rising	–	10	ns
7	Delay CHICLK Falling to CHIFS(Master)	Falling	–	10	ns
4	Delay CHICLK Rising to CHIDOUT(Slave)	Rising	–	15	ns
4	Delay CHICLK Rising to CHIDOUT(Slave)	Falling	–	15	ns
7	Delay CHICLK Falling to CHIDOUT(Slave)	Rising	–	15	ns
7	Delay CHICLK Falling to CHIDOUT(Slave)	Falling	–	15	ns
4	Delay CHICLK Rising to CHIFS(Slave)	Rising	–	15	ns
4	Delay CHICLK Rising to CHIFS(Slave)	Falling	–	15	ns
7	Delay CHICLK Falling to CHIFS(Slave)	Rising	–	15	ns
7	Delay CHICLK Falling to CHIFS(Slave)	Falling	–	15	ns
5	CHIDIN to CHICLK Rising Setup time(Master)	–	20	–	ns
6	CHIDIN to CHICLK Rising Hold time(Master)	–	20	–	ns
8	CHIDIN to CHICLK Falling Setup time(Master)	–	20	–	ns
9	CHIDIN to CHICLK Falling Hold time(Master)	–	20	–	ns
5	CHIFS to CHICLK Rising Setup time(Slave)	–	20	–	ns
6	CHIFS to CHICLK Rising Hold time(Slave)	–	20	–	ns
8	CHIFS to CHICLK Falling Setup time(Slave)	–	20	–	ns
9	CHIFS to CHICLK Falling Hold time(Slave)	–	20	–	ns
5	CHIDIN to CHICLK Rising Setup time(Slave)	–	20	–	ns
6	CHIDIN to CHICLK Rising Hold time(Slave)	–	20	–	ns
8	CHIDIN to CHICLK Falling Setup time(Slave)	–	20	–	ns
9	CHIDIN to CHICLK Falling Hold time(Slave)	–	20	–	ns



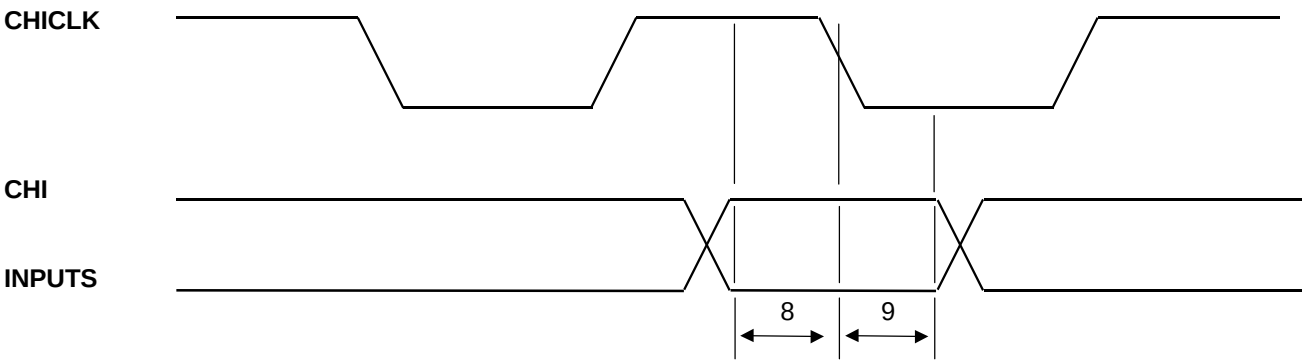
CHI Output and Clock Timing (CHITXEDGE=1)



CHI Input Timing (CHIRXEDGE=1)



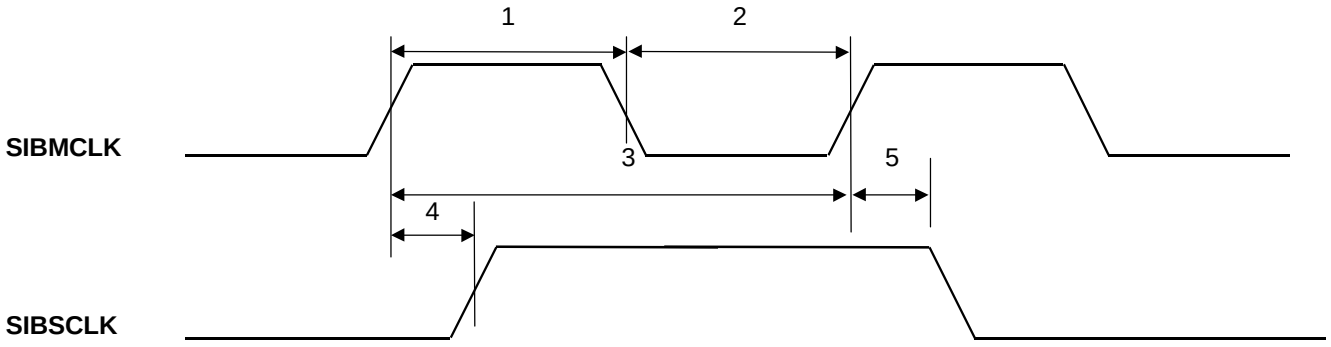
CHI Output and Clock Timing (CHITXEDGE=0)



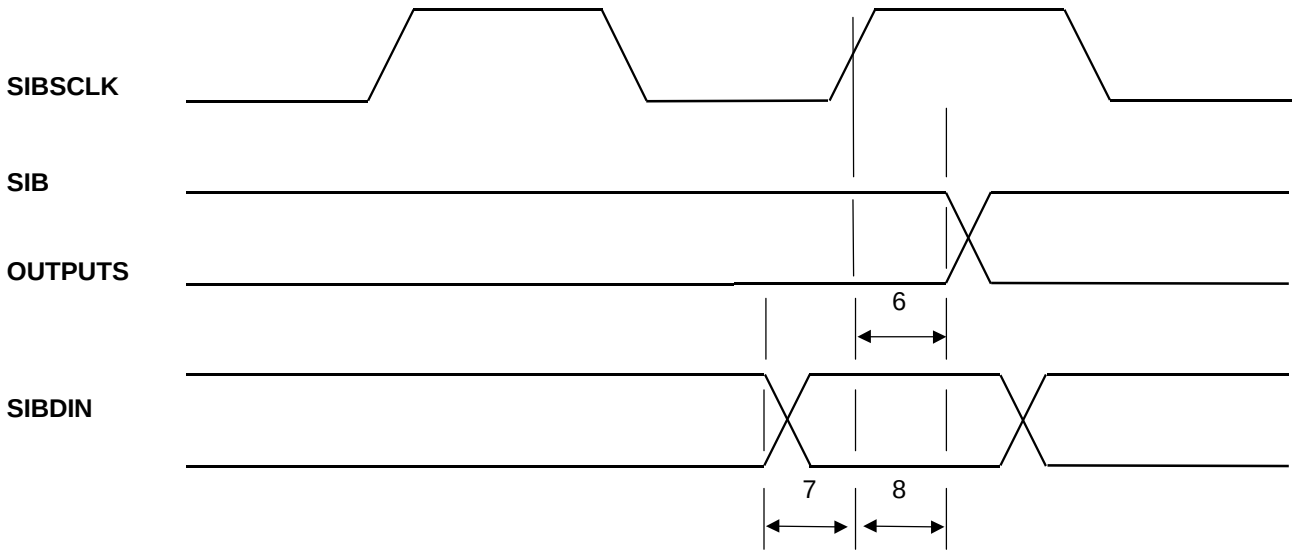
CHI Input Timing (CHIRXEDGE=0)

<SIB>

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	SIBMCLK high time	–	20	–	ns
2	SIBMCLK low time	–	20	–	ns
3	SIBMCLK period	–	50	–	ns
4	Delay SIBMCLK (Master) to SIBSCLK	Rising	–	10	ns
5	Delay SIBMCLK (Master) to SIBSCLK	Falling	–	10	ns
6	Delay SIBSCLK Rising to SIBSYNC	Rising	–	10	ns
6	Delay SIBSCLK Rising to SIBSYNC	Falling	–	10	ns
6	Delay SIBSCLK Rising to SIBDOUT	Rising	–	10	ns
6	Delay SIBSCLK Rising to SIBDOUT	Falling	–	10	ns
7	SIBDIN to SIBSCLK Rising Setup time	–	20	–	ns
8	SIBDIN to SIBSCLK Rising Hold time	–	0	–	ns



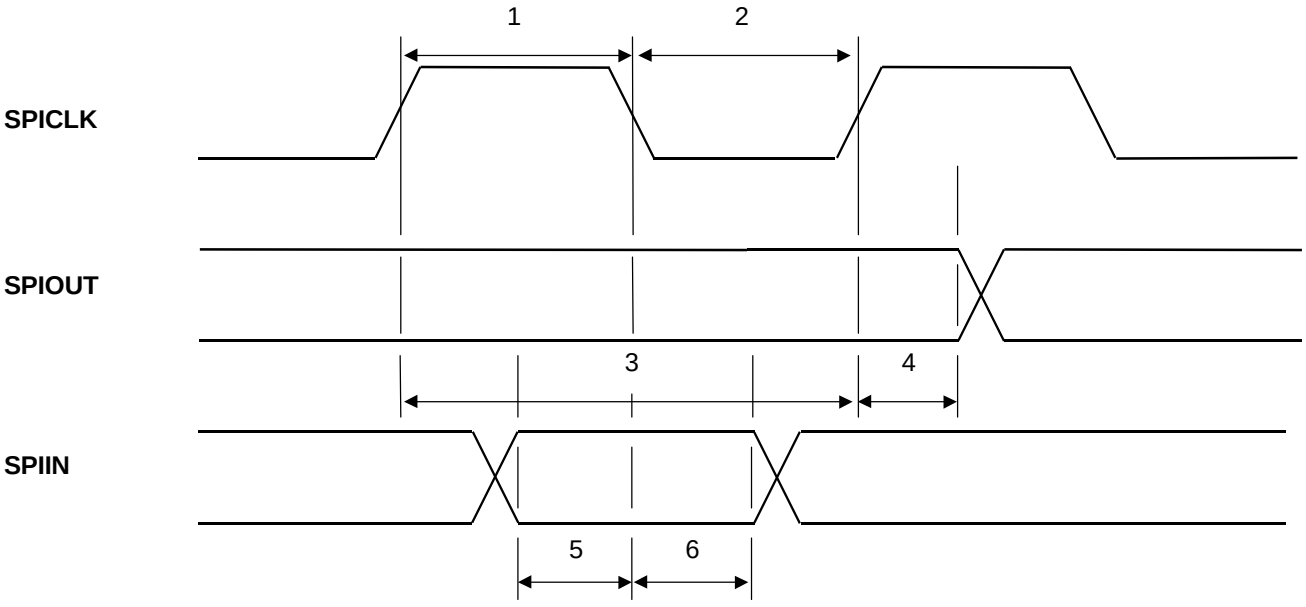
SIB CLK Timing



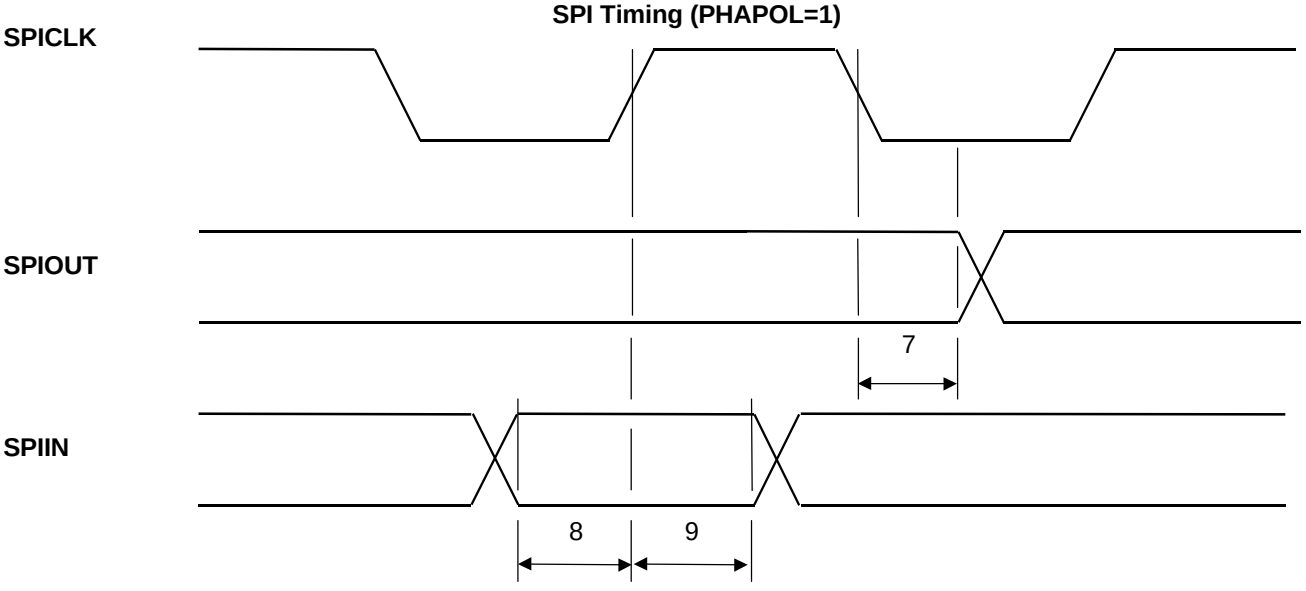
SIB Timing

<SPI>

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	SPICLK high time	–	120	–	ns
2	SPICLK low time	–	120	–	ns
3	SPICLK period	–	250	–	ns
4	Delay SPICLK Rising to SPIOUT	Rising	–	10	ns
4	Delay SPICLK Rising to SPIOUT	Falling	–	10	ns
7	Delay SPICLK Falling to SPIOUT	Rising	–	10	ns
7	Delay SPICLK Falling to SPIOUT	Falling	–	10	ns
8	SPIIN to SPICLK Rising Setup time	–	15	–	ns
9	SPIIN to SPICLK Rising Hold time	–	15	–	ns
5	SPIIN to SPICLK Falling Setup time	–	15	–	ns
6	SPIIN to SPICLK Falling Hold time	–	15	–	ns



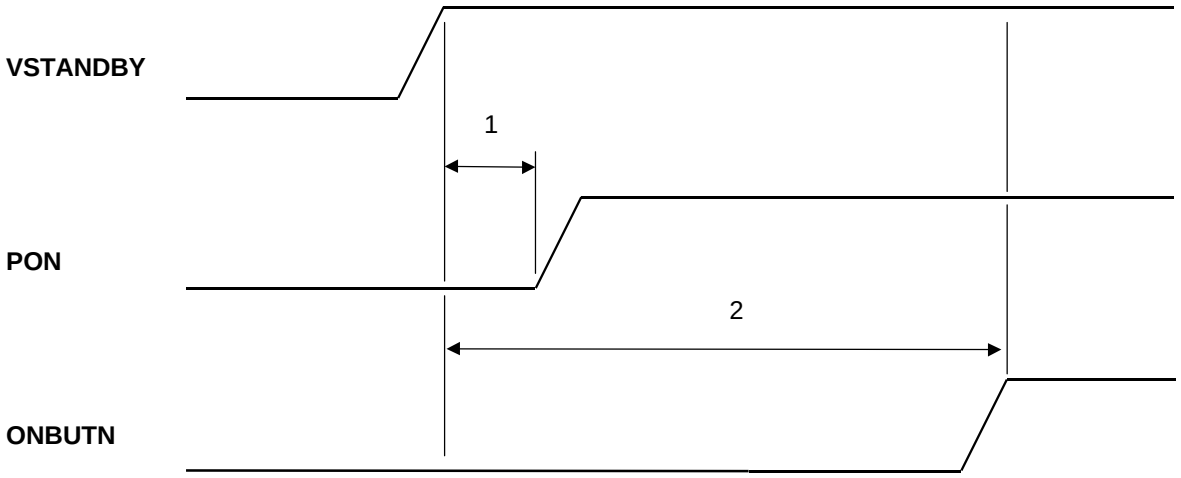
SPI Timing (PHAPOL=1)



SPI Timing (PHAPOL=0)

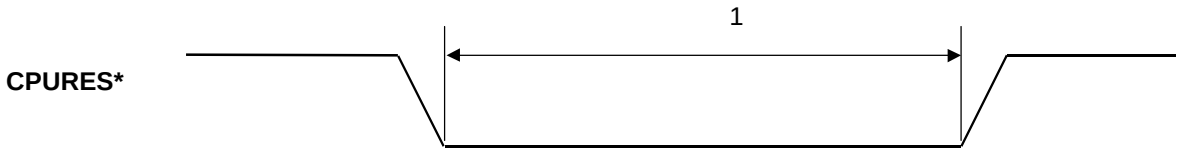
<POWER>

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	VSTANDBY to PON* Rising	–	50	–	ms
2	VSTANDBY to ONBUTN delay time	–	2	–	s



<CPU RESET>

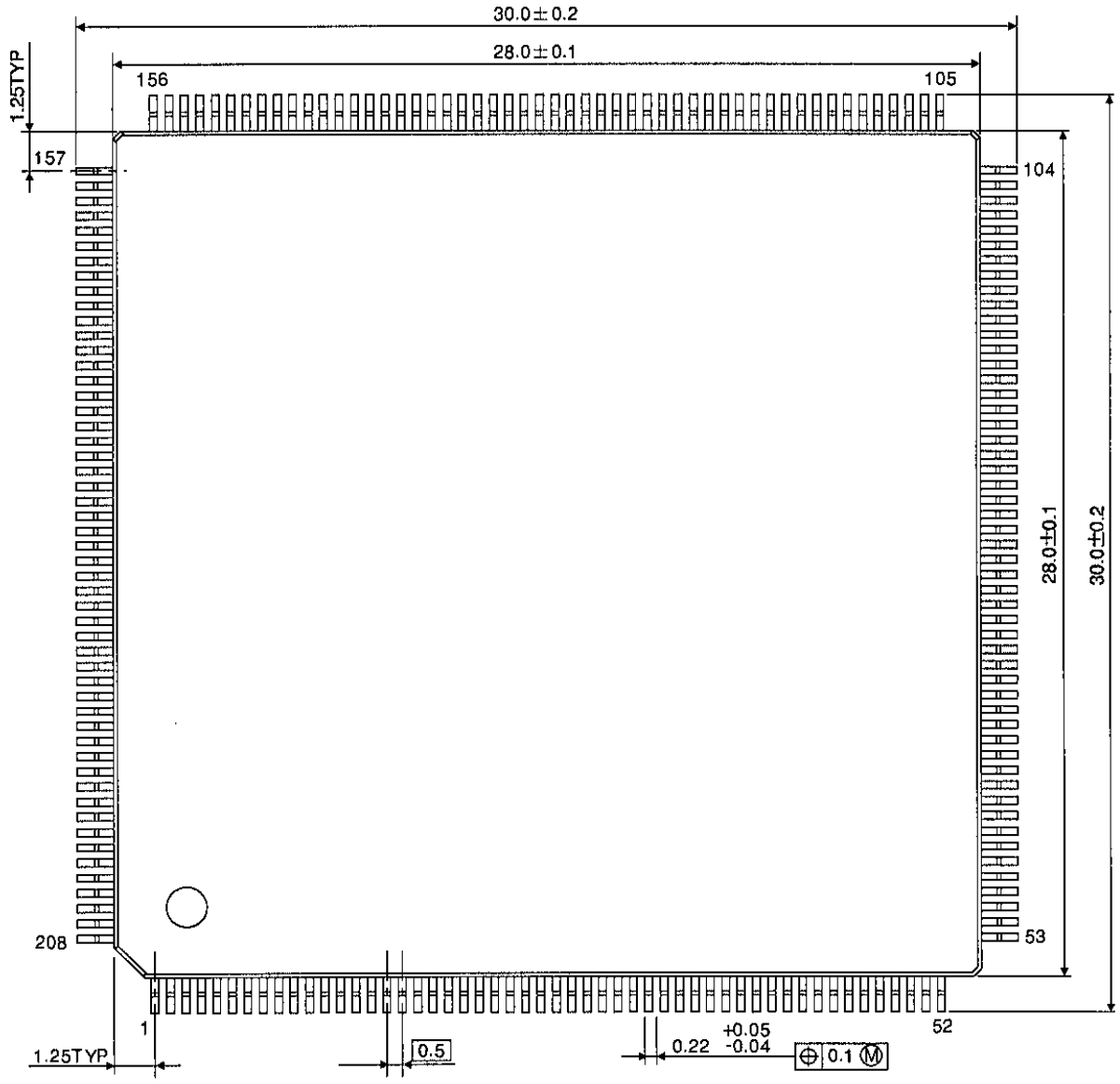
Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	CPURES* low time	–	10	–	ns

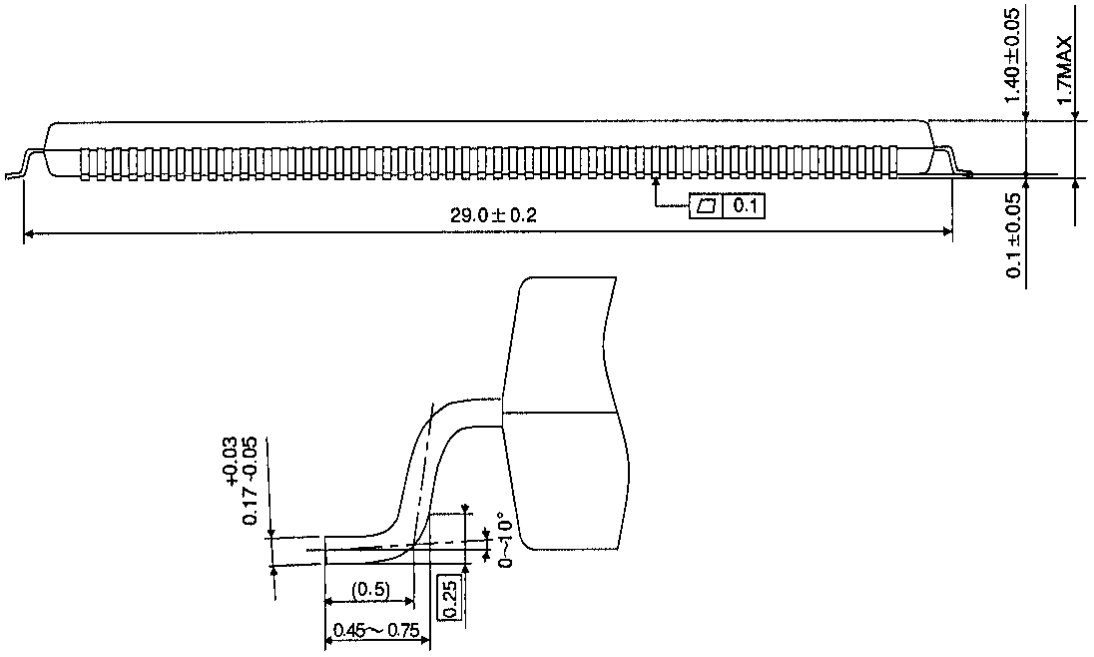


7. PACKAGE DIMENSION

7.1 TMPR3922AU

LQFP208-P-2828-0.50A Unit : mm




1.40±0.05
1.7MAX
29.0±0.2
0.1
0.1±0.05
+0.03
0.17 -0.05
0~10°
(0.5)
0.45~0.75
0.25